(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 360 442 A1**

(12) **EUROPEAN PATENT APPLICATION**

(21) Application number: **89308858.3**

(22) Date of filing: **01.09.89**

(51) Int. Cl.5: **H03L 7/189 , H03L 7/14**

(30) Priority: **02.09.88 JP 218586/88**
**07.10.88 JP 254199/88**
**18.11.88 JP 291999/88**

(43) Date of publication of application:
**28.03.90 Bulletin 90/13**

(84) Designated Contracting States:
**DE FR GB SE**

(71) Applicant: **Nippon Telegraph and Telephone Corporation**
**1-6 Uchisaiwaicho 1-chome Chiyoda-ku**
**Tokyo 100(JP)**

(72) Inventor: **Tarusawa, Yoshiaki**
**4622-3-A-404, Kamariya-cho Kanazawa-ku**
**Yokohama-shi Kanagawa 236(JP)**
Inventor: **Saito, Shigeki**
**1-28-D-909, Deiki Kanazawa-ku**
**Yokohama-shi Kanagawa 236(JP)**
Inventor: **Yamao, Yasushi**
**510-7-5-101, Tsukui**
**Yokosuka-shi Kanagawa 239(JP)**
Inventor: **Nojima, Toshio**
**2-25-13 Hairando**
**Yokosuka-shi Kanagawa 239(JP)**

(74) Representative: **Darby, David Thomas et al**
**Abel & Imray Northumberland House 303-306**
**High Holborn**
**London WC1V 7LH(GB)**

(54) **Frequency sythesizer.**

(57) The oscillation frequency of a voltage controlled oscillator (4) is controlled by setting a division ratio of a variable ratio divider (2) provided in a feedback path of a phase locked loop. When the frequency is switched by changing the division ration a steering voltage (Vda) is applied to the voltage controlled oscillator. This steering voltage can compensate non-linearity so as to reduce the frequency errors and phase errors after switching to thereby enable high speed frequency switching.

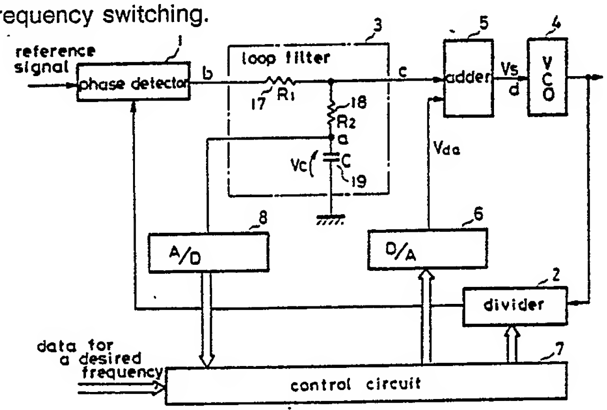



FIG. 7

# FREQUENCY SYNTHESIZER

[Technical Field]

This invention relates to a frequency synthesizer to be used for multichannel access type systems. More particularly, this invention relates to a frequency synthesizer which has a high frequency stability and a low phase noise, and is capable of high speed switching of oscillation frequency. More specifically, this invention relates to a frequency synthesizer which is constructed to use a phase-locked loop (PLL), and is adapted to supply a steering voltage to a voltage-controlled oscillator from outside of the phase locked loop (PLL) at the oscillation frequency switching in order to shorten the settling time of PLL.

This invention is suitable for application as a local oscillator or a carrier oscillator in a radio transmitter/receiver.

[Background Technology]

Frequency domain multichannel access system is widely used in recent years to satisfy a large number of call requests without failure and to increase utilization efficiency of frequencies. The multichannel access system is characterized in that a large number of channels are used to construct the system which is allocated to a large number of subscribers so that a subscriber may use a vacant channel within the system for his/her call. This system requires a frequency synthesizer which is capable of switching a large number of frequencies easily. It is desirable to reduce the time required for frequency switching in order to realize non-interruption h andover during the communication.

Frequency synthesizer using PLL (phase-locked loop) is currently the most prevailing type. A PLL frequency synthesizer phase-locks the output signals from a voltage controlled oscillator (VCO) and the output signals from a reference oscillator. Therefore, is a reference oscillator with a high frequency stability is used, an output with extremely stable frequency can be obtained in the static state. Frequency is switched by changing the division ratio set at a frequency divider inside the PLL. The time required for switching frequencies of PLL frequency synthesizer is determined by the closed-loop bandwidth which is dependent on the reference frequency, phase detector gain, etc. Especially when output frequencies spacing has to be set narrowly, closed-loop bandwith cannot be increased, because the division ratio requirs a large value.

Frequency switching of PLL frequency synthesizer and the conventional method for reducing the time of frequency switching will be described below.

FIG. 1 is a block diagram to show the construction of a conventional PLL frequency synthesizer. The frequency synthesizer comprises a phase detector 1, a variable ratio divider 2, a loop filter 3, and a voltage controlled oscillator 4 (hereinafter referred to as VCO). Each circuit forms a phase locked loop PLL) wherein the output phase of VCO 4 is synchronized with the phase of the reference signal in the static state. If it is assumed that the frequency of the reference signal is denoted as $f_r$, the output frequency of VCO 4 as $f_o$, and the division ratio of the variable ratio divider 2 as N, the output frequency $f_o$ in the phase locked state (or static state) can be expressed as the equation (1)

$f_o = N^*f_r$ (1)

The output frequency may be switched from $f_{o1}$ to $f_{o2}$ by switching the division ratio from $N_1$ to $N_2$. If a stable reference signal is supplied, plural stable frequencies may be obtained by switching the division ratio set at the divider 2. For isntance, if the reference signal $f_r$ is 12.5 kHz, the output frequency may be step stepwise from 1.60 GHz to 1.625 GHz by varying the division ratio N from 128,000 to 130,000.

FIG. 2 shows an example of transient behaviors of the PLL frequency synthesizer at the frequency switching. More specifically, when the division ratio set at the divider 2 is switched at the time $t_o$, the output frequency needs a certain time (time for switching frequency) before it reaches a target frequency $f_{o2}$. During the transient time, voltage $V_c$ of the capacitor in a loop filter 3 in FIG. 1 changes from $V_{c1}$ to $V_{c2}$ as shown in FIG.2. The frequency switching time needs to include at least the time for charging/discharging the capacitor. For instance, if it is assumed that the output frequency is in the 1.6 GHz band and the refer ence signal frequency is 12.5 kHz, the time required is in the range of 50 ms.

In order to reduce the frequency switching time, there has been proposed a frequency synthesizer having the construction shown in FIG. 3. The construction differs from that of the synthesizer of FIG. 1 in that it is provided with a D/A converter 6 and an adder 5. The adder 5 outputs the sum of the output voltage $V_{da}$ of the D/A converter 6 and the output from the loop filter 3 as the output in steering voltage $V_s$ of VCO

4. As no electric current passes through the resistors $R_1$ and $R_2$ in FIG. 3 in the static state, the voltages $V_c$ of the capacitor becomes identical to the output from the loop filter 3. Accordingly, the steering voltage Vs of VCO 4 can be expressed by the equation (2)

$V_s = V_c + V_{da}$ (2)

It is assumed that the current output frequency is denoted as $f_{o1}$, and the steering voltage for VCO 4 correponding thereto as $V_{s1}$ . If the relation $V_{da} = V_{s1}$ holds, it will hold that $V_c = 0$. If the frequency is to be switched from $f_{o1}$ to $f_{o2}$, the division ratio of the variable ratio divider 2 should be switched from $N_1$ to $N_2$. In the static state after switching, the VCO controlling voltage corresponding to the frequency $f_{o2}$ is assumed to be $V_{s2}$ , and if the relation $V_{da} = V_{s2}$ is set as soon as the division ratio is switched, the relation $V_c = 0$ holdsor the voltagr of the capacitor staysat the 0 volt. This reduces the charging/discharging time of the capacitor in the loop filter. The transient behavior would be the same as that of the construction shown in FIG. 1 if the voltage Vda is unchanged despite the frequency switching. By using the construction of FIG. 3, the time necessary to switch frequency is shortened as shown in FIG. 4.

The operation will be further analyzed below. In VCO, the relation between the output frequency f and the steering voltage $V_s$ is varied due to changes in temperature, etc. It is assumed that the behavior at the time of frequency switching shows linear voltage controlled characteristics as shown in Fig. 5. The frequency variation of VCO is extreme small compared to the oscillation frequency, and the frequency drift $\Delta f_o$ could be regarded constant irrespective of the steering voltage $V_s$ . In FIG. 5, at the time $t = t_o$, and when the output frequency $f_o$ is $f_{o1}$, the steering voltage $V_s$ would be $V_{s1}$ . When the output frequency of VCO changes by the drift $\Delta f_o$, the steering voltage $V_s$ decreases by the drift compensation voltage $\Delta V_s$ by the operation of PLL so as to maintain the output frequency at $f_{o1}$. More particularly, drift compensation voltage $-\Delta V_c$ ($= -\Delta V_s$) necessary to compensate the frequency drift $\Delta f_o$ is generated at the capacitor in the loop filter. The output frequency can be fast switched from $f_{o1}$ to $f_{o2}$ by setting a steering voltage $V_{s2}$ at the D/A converter disregarding the drift compensation voltage $\Delta V_c$. The VCO steering voltage is set at a value corresponding to a desired frequency ($V_{s2} - \Delta_{Vs}$). In this way, frequency may be switched without changing the voltage at the capacitor.

However, even though the frequency change is maintained constant irrespective of the steering voltage, the relation between the steering voltages of VCO and the output frequencies $f_o$ is not necessarily linear as shown in FIG. 5. For instance, the electrical tuning capacitor C of the VCO is made by a varactor diode. In this case, the drift compensation voltage $\Delta V_{s1}$ caused by the frequency drift $\Delta f_o$ at $f_{o1}$ is different from the drift compensation voltage $\Delta V_{s2}$ at $f_{o2}$ as shown in FIG. 6. Therefore at the frequency switching, if the steering voltage $V_{s2}$ is at as it is, there will be caused errors equivalent to the difference of the drift compensation voltages $\Delta V_{s1}$ and $\Delta V_{s2}$, and PLL works to charge/discharge te capacitor in order to compensate the difference. Therefore, the time required for frequency switching is not quite reduced heretofore.

Moreover, the reference signal phase and the output phase of the variable ratio divider do not always agree immediately after the controlling voltage data is set in the D/A converter. PLL works to cancel the phase errors to thereby vary the output frequency as shown in FIG. 4.

Because of those reasons, the time required for frequency switching could not heretofore be reduced beyond a certain time.

This invention was conceived to eliminate such problems encountered in the prior art and aims to provide a frequency synthesizer which is capable of high speed switching of oscillation frequency.

[Disclosure of the Invention]

According to the first aspect of this invention, there is proposed a frequency synthesizer which measures frequency controlling voltage of a voltage-controlled oscillator and corrects the errors of the oscillation frequency after switching based on the measured value.

More particularly, this invention provides a frequency synthesizer which includes a voltage controlled oscillator, a variable ratio divider which divides the output from the oscillator, a phase detector which compares the output phase from the variable ratio divider with the phase of the reference signal, a loop filter which smoothens the output from the detector and supplies the same to said voltage controlled oscillator, and an oscillation frequency switching means which switches the oscillation frequency of said oscillator by changing the division ratio of said variable ratio divider wherein said oscillation frequency switching means includes a voltage supply means which supplies a steering voltage of said voltage controlled oscicllator orresponding to the oscillation frequency after switching to said voltage controlled oscillator via the D/A converter in synchronization with the change of the division ratio of said divider. This invention synthesizer

is characterized in that said voltage controlled oscillator is an oscillator of which frequency changes non-linearly in respect of input steering voltage, and which includes a voltage measurement means which measures by means of an A/D converter the volt age which has been supplied to said voltage controlled oscillator through said loop filter before switching of the oscillation frequency, and said voltage supply means includes a steering voltage correction means which corrects the steering voltage to be supplied to said voltage conrolled oscillator based on said value measured by said voltage measurement means correspondingly to the non-linearity of the voltage controlled oscillator.

The steering voltage correction means preferably includes a means which adds to the output from said loop filter a voltage value which is expressed as below,

$V_{s2} - (\Delta V_{s2} - \Delta V_{s1})$

wherein the value obtained by the voltage measurement means is represented as $\Delta V_{s1}$, the drift in oscillation frequency of said voltage controlled oscillator caused by the voltage $-\Delta V_{s1}$ as $\Delta f_o$, the steering voltage coresponding to the oscillator frequency after switching as $V_{s2}$, and the voltage required to vary the oscillator frequency of said oscillator after switching of the frequency the amount of $\Delta f_o$ as $- \Delta V_{s2}$.

The second aspect of this invention provides a frequency synthesizer which does not cause phase errors substantially between the reference signal and the output from the divider by triggering the reference signal to reset the variable ratio divider.

More particularly, the frequency synthesizer includes a voltage controlled oscillator, a variable ratio divider which divides the frequency of the output from the voltage controlled oscillator, a phase detector which compares the output phase of the variable ratio divider with the phase of the reference signal, a loop filter which smoothens the output from the detector and supplies it to said voltage controlled oscillator, and an oscillation frequency switching means which switches the frequency oscillated by said voltage controlled oscillator varying the division ratio of the variable ratio divider, wherein the switching means includes a voltage supply means which supplies a steering voltage corresponding to the oscillation frequency after switching in synchronization with the changes of dividing ratio of said divider to said voltage controlled oscillator via the D/A converter. This invention synthesizer is characterized in that said variable ratio divider is a variable ratio divider with a reset means, and the oscillation frequency switching means includes a means which is triggered by the reference signal inputted at the phase detector to reset said variable ratio divider.

The loop filter is preferably provided with a loop switch at an output thereof, and the oscillation frequency switching means preferably includes a switch ON/OFF means which opens said loop switch before switching the oscillation frequency and closes it after the variable ratio divider is reset.

It is most desirable to have both the first and second aspects of this invention concurrently.

The frequency synthesizer having either one or both in combination of the first and the second aspects of the invention may include a means which stops the power supply to said D/A converter after a sample hold circuit is connected to the output of the D/A converter and a steering voltage is held at the circuit.

The sample hold circuit includes a capacitor which may be the same capacitor which is an element of the loop filter.

A variable bandwidth filter may be connected to an output of the D/A converter, and the oscillation frequency switching means may include a bandwidth controlling means which narrows the bandwidth of said variable bandwidth filter after switching the oscillation frequency. Separately from the above, a variable bandwidth filter is connected to an input of the voltage controlled oscillator, and the oscillation frequency means may include a bandwidth controlling means which narrows the bandwidth of the filter after switching the oscillation frequency.

The output of the D/A converter may be connected to a low-pass filter to include a means which sequentially sets plural different voltages before the steering voltage corresponding to the frequency after the switching is set at the output of the D/A converter.

According to the first aspect of this invention the frequency errors can be reduced effectively, and phase errors can be absorbed according to the second aspect thereof.

As the steering voltage is generated in a manner not to vary the output voltage of the loop filter in the first aspect of this invention, and the variable ratio divider is reset at the time of frequency switching in the second aspect thereof, the phase errors which might be caused otherwise at the switching can be reduced.

Accordingly, due to the advantages achieved by the first and the second aspects of this invention, the time necessary to switch frequency can be remarkably shortened.

When a variable bandwidth filter is used, the bandwidth should be set wider at the time of switching oscillation frequency, and narrower after settling. This enables the supply of steering voltage with a quick rising at the time of switching, and after the oscillation frequency changes, prevents the noise of the D/A converter provided within the voltage supply means from being transmitted to the voltage controlled

oscillator.

The same effect may be obtained by separating the D/A converter from the phase-locked loop after frequency switching. In this case, the capacitor of the loop filter is used as the sample hold circuit.

In other words, the digital-analog converter which deteriorates noise characteristics of the voltage controlled oscillator is separated from the phase locked loop except during the time of frequency switching. This enables frequency switching at a higher speed and prevents deteriortion in noise characteristics of the voltage controlled oscillator at static state.

The frequency synthesizer of the type is most effective when applied to radio communication systems which switch plural radio channels. Such system is required to search vacant channels at a high speed or switch radio channels without interrupting the communication. By using the frequency synthesizer of this invention as a local oscillator for such radio communication systems, stable locally oscillated frequency may be obtained, and radio channels may be switched at high speed. Moreover, as this allows vacant channel search and non-interrupted channel switching without difficulties, it is highly effective to enhance functions and the performance of the systems.

[Brief Description of the Drawings]

FIG. 1 is a block diagram of a conventional frequency synthesizer.

FIG. 2 is a graph to shown an example of transient behaviors of PLL frequency synthesizer at the time of switching.

FIG. 3 is a block diagram of another conventional frequency synthesizer.

FIG. 4 is a graph to show variation in output frequency of the voltage controlled oscillator in relation to the changes in output voltage from a D/A converter.

FIG. 5 is a graph to show an example of characteris tics of the output frequency in relation to the steering voltage of the voltage controlled oscillator.

FIG. 6 is a graph to show another example of the characteristics of the output frequency in relation to the steering voltage of the voltage controlled oscillator.

FIG. 7 is a block diagram to show the first embodiment of the frequency synthesizer according to this invention.

FIG. 8 is a block diagram to show the second embodiment of the frequency synthesizer according to this invention.

FIG. 9 is a block diagram to show the third embodiment of the frequency synthesizer according to this invention.

FIG. 10 is a block diagram to show the fourth embodiment of the frequency synthesizer according to this invention.

FIG. 11 is a chart to explain timings at frequency switching.

FIG. 12 is a block diagram to show the fifth embodiment of the frequency synthesizer according to this invention.

FIG. 13 is a block diagram to show the sixth embodiment of the frequency synthesizer according to this invention.

FIG. 14 is a view to show an embodiment of the phase detector which has a loop switching function.

FIG. 15 is a block diagram to show an embodiment of the internal construction of a control circuit.

FIG. 16 is a block diagram to show another embodiment of the internal construction of the control circuit.

FIG. 17 is a block diagram to show the seventh embodiment of the frequency synthesizer according to this invention.

FIG. 18 is a circuit diagram to show an embodiment of a variable bandwidth filter.

FIG. 19 is a circuit diagram to show an embodiment of a voltage controlled resistor.

FIG. 20 is a block diagram to show the eighth embodiment of the frequency synthesizer according to this invention.

FIG. 21 is a block diagram to show the ninth embodiment of the frequency synthesizer according to this invention.

FIG. 22 is a block diagram to show the tenth embodiment of the frequency synthesizer according to this inven tion.

FIG. 23 is a block diagram to show the details of the tenth embodiment.

24. is a chart to show timings at frequency switching.

FIG. 25 is a block diagram to show a voltage controlled oscillator and the circuit construction for

controlling it.

FIG. 26 is a block diagram to show another voltage controlled oscillator and a circuit construction for controlling it.

FIG. 27 is a graph to show transient behavior of the VCO controlled circuit of FIG. 25 at the time of frequency switching.

FIG. 28 is a block diagram to show the first embodiment of the VCO controlling circuit.

FIG. 29 is a chart to show the waveforms of the output voltage from the D/A converter and the changes in output frequency of the VCO.

FIG. 30 is a circuit diagram to show the construction of the first order low-pass filter.

FIG. 31 is a chart to show transient behavior of the VCO controlling circuit when the first order low-pass filter is used.

FIG. 32 is a view to show the transient behavior when the output from the D/A converter is saturated.

FIG. 33 is a block diagram to show the first embodiment of the VCO controlling circuit.

FIG. 34 is a view to show the frequency switching characteristics in the conventional embodiment shown in FIG. 1.

FIG. 35 is a view to show the frequency switching characteristics in the embodiment shown in FIG.10.

[Optimal Mode for Embodying This Invention]

FIG. 7 is a block diagram to show the first embodiment of frequency synthesizer according to this invention. The embodiment differs from the prior art shown in FIG. 3 in that the voltage $V_c$ of the capacitor is taken out by an A/D converter 8 and the data thereof is supplied to a control circuit 7. Errors in set voltage which heretofore are caused in the prior art can be avoided by construction mentioned above. For instance, when the steering voltage vs. output frequency characteristics are not linear as shown in the VCO in FIG. 6, the drift compensation voltage $\Delta V_s$ corresponding to the frequency drift $\Delta f_o$is different between the steering voltages $V_{s1}$ and $V_{s2}$ as indicated in the voltages $\Delta V_{s1}$ and $\Delta V_{s2}$. Therefore, at frequency switching, the frequency drift $\Delta f_o$ is obtained from the values of the drift compensation voltage $\Delta V_{s1}$ in advance, a value of drift compensation voltage $\Delta V_{s2}$ is assumed from the frequency drift $\Delta f_o$ and set the value $V_{s2}$ - ($\Delta V_{s2}$ - $\Delta V_{s1}$ ) at the D/A converter 6.

Under the static state, the drift compensation voltage $\Delta V_{s1}$ becomes equal to the voltage of the capacitor, which is taken out by the A/D converter 8. As the frequency drift $\Delta f_o$ is extremely small, it is obtainable from the VCO gain in the steering voltage $V_{s1}$ and the drift compensating voltage $\Delta V_{s2}$. The voltage drift $\Delta V_{s2}$ may be assumed from the frequency drift $\Delta f_o$ and the VCO gain of the steering voltage $V_{s2}$.

As described above, by setting the output of the D/A converter Vda corresponding to the output frequency $f_{o2}$ as $V_{s2}$ - ($\Delta V_{s2}$ - $\Delta V_{s1}$) and adding the same to an adder 5 at the same time as the division ratio is changed, the frequency can be switched without changing the voltage of the capacitor.

FIG. 15 is a block diagram to show the internal construction of such control circuit 7 wherein a ROM table 17 stores steering voltage vs. VCO output frequency characteristics before the drift shown with solid lines in FIG. 6, inputs desired frequency data, and outputs steering voltage data $V_s$ corresponding thereto. A drift compensation circuit 70 calculates frequency drift $\Delta f_o$ and drift compensation voltage $\Delta V_{s1}$ from the out of the Vda supplied to the D/A converter 6 and the $V_c$ data which is an output from the A/D converter 8, and stores the result, obtains the voltage drift $\Delta V_{s2}$ corresponding to the frequency $f_{o2}$ by referring to the table when the desired frequency data is shifted from $f_{o1}$ to $f_{o2}$, and outputs the drift compensation voltage $\Delta V_s$ = $\Delta V_{s2}$ - $\Delta V_{s1}$ . A subtractor 72 supplies steering voltage $V_{ss}$ = $V_{s2}$ - ($\Delta V_{s2}$ - $\Delta V_{s1}$) to a latch for D/A data 73. ROM table 71 supplies the the voltage $V_{s2}$ corresponding $f_{o2}$. ROM 75 for division ratio receives as input a desired frequency data and supplies division ratio data corresponding thereto a latch for division ratio 74. When switching the desired frequency data from $f_{o1}$ to $f_{o2}$, a timing circuit 76 supplies latch signals respectively to the latch 73 for D/A data and the latch 74 for division ratio after completion of arithmetic operation by the subtractor 72. This renews Vda data and the division ratio data.

Frequency switching time can be shortened by the above operation without making errors in steering voltage even though VCO characteristics are not linear. In FIG. 7 the input of the A/D converter is connected to a terminal or point a of the capacitor in order to take out the capacitor voltage $V_c$, but the same effect may be achieved by taking out the voltage at the points b,c and d from the A/D converter 8 instead of the point a as the electric current does not flow through the resistors $R_1$ and $R_2$ in the static state. However, if the voltage is taken out at the point d, the capacitor voltage $V_c$ is calculated by subtracting the voltage Vda from the value which has been taken out.

In the aforementioned embodiment, a sample hold circuit may be connected to an output of the D/A

converter 6 and the steering voltage may be outputted from the sample hold circuit to an adder 4. In this case, power supplying to the D/A converter 6 is stoped after the steering voltage is held at the sample hold circuit. This saves power consumption.

FIG. 8 is a block diagram to show the second embodiment of a frequency synthesizer according to this invention. This embodiment differs from the first embodiment shown in FIG. 7 in that the D/A converter 6 is connected in series to the grounding point of the loop filter 3 to omit the adder. The VCO steering voltage $V_s$ may be expressed similarly to the equation (2) as $V_s = V_c + VDa$ if the voltage of the capacitor is denoted as $V_c$, and the output of the D/A converter as Vda. In this embodiment, $V_c$ + Vda is taken out from the A/D converter 8 and drift compensation voltage $\Delta V_s$ (= $V_c$) may be obtained by subtracting the voltage Vda from the taken out value. Then, frequency drift $\Delta f_o$ is calculated by the manner similar to the first embodiment, and a D/A converter output data suitable to the output frequency $f_{o2}$ which is to be outputted next is set. The effect similar to the first embodiment can be obtained and the circuit structure may be simplified. As no electric current through the resistors $R_1$ and $R_2$ at the static time, the voltage may be taken out at the point $\underline{b}$ or $\underline{c}$ instead of the point $\underline{a}$ by using the A/D converter 8 to attain the same effect.

FIG. 9 is a block diagram to show the third embodiment frequency synthesizer according to this invention. This embodiment differs from the first embodiment shown in FIG. 7 in that a loop filter 9 includes an operational amplifier in the loop filter 9, and the D/A converter output (Vda) is supplied to a non-inverting input of the operational amplifier which is a signal grounding point of the loop filter 9, and the A/D converter 8 is connected to the output of the loop filter.

The steering voltage $V_s$ of VCO 4 may be expressed as $V_s = V_c$ + Vda similarly to the formula (2) if the voltage of a capacitor is represented as $V_c$ and the output of D/A converter Vda. As no electric current through the resistors $R_1$ and $R_2$ in the static state, $V_c$ and Vda may be obtained from the output from the loop filter. Therefore, the effect similar to the second embodiment shown in FIG. 7 may be obtained by subtracting the voltage Vda from $V_c$ + Vda and calculating $\Delta V_s$ (= $V_c$).

FIG. 10 is a block diagram to show the fourth embodi ment of the frequency synthesizer of this invention. Japanese Patent Application Sho 61-305253 has proposed a method to suppress frequency fluctuation caused by phase errors when PLL is operated intermittently. The operation of the proposed method is applied to reduce the phase errors at the frequency switching herein. This embodiment differs from the first embodiment FIG. 7 in that the reference signal is inputted in the control circuit 7 as a trigger signal and the reset signal is sent to the variable ratio divider 2.

FIG. 11 is a chart to show the timings of frequency switching wherein the loop switch 10 is turned OFF to open the loop at the time $t_1$. The output voltage of the D/A converter 6 is turned from Vda1 to Vda2, and the division ratio is shifted from $N_1$ to $N_2$. The steering voltage of VCO 4 is set at a level corresponding to the target frequency at this stage. The reference signal phase may be different from the phase of the variable ratio divider as shown in FIG. 11. If the loop switch 10 is turned ON as it is, the phase error may cause fluctuation in output frequency. In order to inhibit the fluctuation, a reset signal is sent out to the variable ratio divider 2 at the time $t_3$. The timing for reset signalis determined by triggering the reference signal. This makes the phase of the variable ratio divider locked with the phase of the output from the referencve signal, and if the loop switch 10 is turned ON at the time $t_4$, drifts will not be caused in output frequency due to phase errors. The steering voltage data to be set at the D/A converter 6 is calculatedly by the method similar to the one shown in FIG. 7. This operation can reduce both the steering·voltage error and the phase error at the frequency switching .

This chart shows a case where the counting of divider re-start at the end of reset signal which is synchronized with the positive edge of reference signal. The counting of divider may re-start at the end of reset signal which is synchronized with the negative edge of reference signal.

FIG. 16 is a block diagram to show the inside of a control circuit 7 which differs from the structure shown in FIG. 15 by a timing circuit 76. The timing circuit 76 receives the reference signal as a trigger, and outputs the reset signal of the variable ratio divider 2 and the loop switch signal in accordance with the aforementioned timing. These signals are executed in the procedure such as "receiving desired frequency data, turning the loop switch OFF, changing Vda and N, sending reset signal, and turning the loop switch ON".

FIG. 12 is a block diagram of the fifth embodiment of the frequency synthesizer according to this invention. This embodiment is a combination of the embodiment shown in FIG. 8 with a reset function of the variable ratio divider 2. As the combined functions can reduce both the steerieng voltage error and phase errors to zero at frequency switching, the effect similar to the embodiment shown in FIG. 10 may be achieved.

FIG. 13 is a block diagram to show the sixth embodi ment of the frequency synthesizer according to this invention. This embodiment is a combination of the embodiment shown in FIG. 9 with a reset function

used for the variable ratio divider in the embodiment shown in FIG. 10. This combination enables reduction of both the steering voltage error and phase errors to zero level at frequency switching to achieve the effect similar to the embodiment shown in FIG. 10.

FIG. 14 shows an embodiment of the phase detector having the loop switch function, and more particularly FIG. 14a shows a basic embodiment of the phase detector having the loop switch function which is used in the embodiments shown in FIGs. 10 through 13. FET analog switches which can be switched at high speed may be used as the loop switch shown in the figures. FIG. 14b shows an embodiment which realizes close/open (ON/OFF) of the phase locked loop by combining a charge pump circuit with an FET analog switch and a logic circuit. In this construction, when "0" of the loop ON/OFF signal is inputted, the output from an OR gate 12 becomes "1" despite the logical output from the digital phase detector 1. P channel FET 15 which uses the output from the OR gate 12 input and an N channel FET 16 which uses the output from an AND gate 13 are opened while the phase locked loop is open. When the loop ON/OFF signal "1" is inputted, the gates of both FETs 15 and 16 are driven with the output of the digital phase detector, the phase locked loop is closed. FIG. 14c shows a loop switch which opens the FET when the digital phase detector 1 is reset. FIG. 14d shows that the loop is opened by holding the input of the circuit 1 with OR gates 12a and 12b so that the logical output from the circuit 1 becomes the same state as the phase locked loop to open FETs 15 AND 16.

In the above embodiments, the output from the D/A converter 6 is used as the steering voltage as it is; however, if noises are included within the output from the D/A converter 6, the noise is directly added to the steering voltage. The phase noise in VCO output increases consequently.

The following embodiments attempt to solve the problems. They can prevent phase noise increase which is caused by the addition of the D/A converter. In the description of the following embodiments, the description on the construction to correct non-linearity of the oscillator 4, structure for resetting variable ratio divider and loop switch will be omitted unless specifically required. FIG. 17 is a block diagram to show the seventh embodiment of the frequency synthesizer according to this invention.

The frequency synthesizer comprises a voltage controlled oscillator 4, a variable ratio divider which divides the output from the oscillator 4, a phase detector 1 which compares the phase of the output from the divider 2 with the phase of the reference signal, a loop filter 3 which smoothens the output from the detector 1 and supplies the same to the oscillator 4, and an oscillation frequency switching means which controls oscillation frequency of the oscillator 4 by switching the division ratio of the divider 2. The oscillation frequency switching means includes a control circuit 7, a digital/analog converter 6 which is a voltage supply means which supplies steering voltage corresponding to the frequency after switching to the oscillator 4 when the division ratio of the divider 2 is switched to vary the oscillation frequency at high speed, a variable bandwidth filter 102 which is connected to the output of the digital analog converter 6 and an adder 5 which adds the output of the variable bandwidth filter 102 with the output from the loop filter 3.

Although the frequency synthesizer includes the circuits shown in relation to the first to the sixth embodiments, description is omitted.

This embodiment is characterized in that the voltage supply means includes a variable bandwidth filter 102, and the control circuit 7 includes a bandwidth limiting means which sets the bandwidth of the filter 102 narrower after the frequency swiching.

The variable bandwidth filter 102 connected to the output side of the D/A converter 6 is set to have a narrow bandwidth at the static state, and therefore does not transmit the noises generated in the converter 6 to the voltage controlled oscillator 4. The bandwidth at this time is denoted as $W_2$.

Description will be given to the case where the frequency is switched from $F_1$ to $F_2$ . the frequency is switched by concurrently conducting changing division ratio of the divider 2, changing of input data of the D/A converter 6 and changing of the bandwidth of the filter 102. These changes are controlled by the control circuit 7.

Concurrently to the data change and division ratio change, the bandwidth of the variable bandwidth filter 102 is shifted from $W_2$ to $W_1$ which is wider than $W_2$. By these procedures, the output voltage of the D/A converter 6 is transmitted to the adder 5 at high speed so that the steering voltage of the oscillator 4 is changed to $V_2$ at high speed, thus enabling high speed frequency switching.

After frequency switching, the bandwidth of the filter 102 is reset at $W_2$ again. This enables to suppress the noise generated by the D/A converter 6 and prevent increase in phase noise characteristics in the output of the oscillator 4.

Therefore, without deteriorating noise characteristics of the oscillator 4, the frequency can be switched at high speed.

FIG. 18 shows an embodiment of the variable bandwidth filter. The filter 102 comprises a voltage controlled resistor 103 which changes resistance by the controlling voltage and a capacitor 104.

FIG. 19 shows an embodiment of the voltage controlled resistor 103. The resistor 103 uses a field effect transistor (FET) which changes resistance between source and drain with the voltage applied in the gate. When the resistance is large, the bandwidth becomes narrow, while the resistance is low, the bandwidth becomes wider.

FIG. 20 is a block diagram to show the eighth embodiment of the frequency synthesizer according to this invention.

This embodiment differs from the seventh embodiment in that the output of the variable bandwidth filter 102 is directly connected to the loop filter 3 in order to add the voltages of the filter 102 and of the loop filter 3. However, the operation thereof is identical to that of the seventh embodiment.

FIG. 21 is a block diagram to show the ninth embodiment of the frequency synthesizer according to this invention.

This embodiment differs from the seventh embodiment in that the variable bandwidth filter 102 is connected between the adder 5 and the voltage controlled oscillator 4, but the operation thereof is identical to that of the seventh embodiment. The bandwidth of the filter 102 is varied at frequency switching in this embodiment. This enables high speed frequency switching without deteriorating the noise characteristics of the oscillator 4.

FIG. 22 is a block diagram to show the tenth embodiment of the frequency synthesizer according to this invention.

In this embodiment the D/A converter 6 is connected to a capacitor in the loop filter 3, and a switch 105 is provided between the D/A converter 6 and the capacitor as a means to disconnect the D/A converter 6 after the steering voltage from the converter 6 is holded in the capacitor.

The switch 105 is open by the control circuit 7 in the static state to disconnect the D/A converter 6 from the loop filter 3. The phase locked loop operates ordinarily in this stage, and the VCO output signal with the stability similar to the output signal from the reference oscillator 101 is obtained from the oscillator 4 in the frequency corresponding to the division ratio N set at the variable ratio divider 2.

Description is now given to the case where the frequency $F_1$ is switched to the frequency $F_2$.

Before switching, the voltage V of the capacitor in the loop filter 3 in the static state after switching of the frequency is set at the D/A converter 6. Then, the division ration $N_2$ is set by the control circuit 7 at the divider 2 in correspondence to the frequency F to which the frequency is going to be switched, and at the same time, the switch 105 is closed to apply the output voltage $V_2$ of the digital analog converter 6 to the capacitor in the loop filter 3. This makes the capacitor charged rapidly, and the frequency of the oscillator 4 is rapidly switched to the frequency $F_2$ . Then, the switch 105 is opened after the completion of charging of the capacitor, so as to cut off the output from the converter 6 from the loop filter 3.

The output from the D/A converter 6 is directly connected to the capacitor of the loop filter 3 via the switch 105. If the output impedance of the D/A converter 6 is sufficiently low, the capacitor can be charged at an extremely high speed. As the D/A converter 6 is disconnected from the loop filter 3 after completion of charging, noises generated from the D/A converter 6 is also blocked without influencing the VCO steering voltage. Therefore, the frequency can be switched at a high speed without deteriorating the noise characteristics of the oscillated signals. The switch 105 may be a variable resistor as it is a circuit to disconnect the signal from the D/A converter 6.

FIG. 23 is a block diagram to show the variation of the tenth embodiment. In this embodiment of the frequency synthesizer, similar to the fourth embodiment shown in FIG. 10, the frequency can be switched at a high speed. Moreover, this enables to suppress the noise generated by D/A converter and prevent increase in phase noise characteristics in the output of the oscillator.

The variable ratio divider 2 is a divider with a reset means, and the control circuit 7 resets the divider 2 using the reference signal inputted at the detector as a trigger.

FIG. 24 is a timing chart to show the timing of frequency switching in FIG. 23 wherein all the timings except for that of the signal controlling the switch 105 are the same as those shown in FIG. 11. In this chart, the counting of divider 2 re-start at the end of reset signal which is synchronised with the positive edge of reference signal.

In the seventh to the tenth embodiments, a variable bandwidth filter or a switch is connected to the output of the D/A converter in order to effect both suppression of output noises from the converter and rapid setting of voltages. The construction may be one where the bandwidth of the filter connected to the output of the D/A converter is fixed to achieve a high speed in voltage setting, which will be explained below.

FIGs. 25 and 26 show circuit structures of the voltage controlled oscillator and a circuit for controlling it. VCO control circuit comprises a ROM 201 and a D/A converter 6 in the circuit 7 so that the voltage outputted from the D/A converter 6 is connected either directly (FIG. 25) or via a low-pass filter 202 (FIG. 26).

In the circuit shown in FIG. 25, the ROM 201 receives desired frequency data as an input from outside and supplies frequency control voltage data corresponding to the desired frequency. This makes frequency control voltage supplied to the VCO 4 correspondingly to the desired frequency. The time necessary to switch frequency becomes equal to the voltage settling time of the D/A converter 6, which can be set to the order of micro seconds if a sophisticated D/A converter is used.

However, as the output of the D/A converter 6 contains the noise voltage, the phase-noise characteristic of the output from VCO 4 may deteriorate. As the noise component in the output from the D/A converter 6 is mostly white noises, as shown in FIG. 26, a low-pass filter 202 is con nected to the output of the converter 6. This suppresses the phase noise, but the frequency switching time becomes longer.

FIG. 27 shows transient behavior characteristics of the VCO circuit shown in FIG. 25, wherein the frequency is switched from $f_a$ to $f_b$. The voltages $V_a$ and $V_b$ are frequency control voltages respectively corresponding to the frequencies $f_a$, and $f_b$. FIG. 27 shows a case were the output voltage from the D/A converter 6 is switched from $V_a$ to $V_b$ stepwise at the time $t_o$. As illustrated in the figure, when a low-pass filter 202 is inserted, frequency control voltage changes gradually in contrast to the output voltage from the D/A converter 6 which rapidly changes.

In order to eliminate such inconvenience, the bandwidth of the low-pass filter 202 is made variable in the seventh to tenth embodiments. Another approach will be shown below.

FIG. 28 is a block diagram to show the first embodiment of a VCO control circuit. The VCO control circuit comprises a ROM 201, an adding data circuit 203, a digital adder 204, and a D/A converter 6. The output from the D/A converter 6 is supplied to the VCO 4 via the low-pass filter 202.

FIG. 29 shows the changes in the output waveform of the D/A converter 6 and in the output frequency of the VCO 4 when the switching operation starts at the $t_o$ to switch the frequency from $f_a$ to $f_b$. The voltages $V_a$ and $V_b$ are VCO control voltages respectively in correspondence to the frequencies $f_a$ and $f_b$. As shown in the figure, in the VCO control circuit, the input voltage of the low-pass filter 202 (or the output voltage of the D/A converter 6) changes from the initial voltage $V_a$ to the target voltage $V_b$ via the voltages $V_1$ and $V_2$. The frequency switching time may be shortened by controlling the input voltage of the low-pass filter 202 to reach the target voltage via plural voltages. In this embodiment, adding data corresponding to such plural voltages $V_1$ and $V_2$ may be obtained by the arithmetic operation by the circuit 203 shown in FIG. 28. The adding data processed by the circuit 203 are sequentially sent to the digital adding circuit 204. The above operation can control the output voltage of the D/A converter 6 to change from the initial voltage $V_a$ to the target voltage $V_b$ via plural voltages $V_1$ and $V_2$.

The arithmetic operation of adding data at the circuit 13 will not be described. This arithmetic operation is based on the optimal control theory which uses the state-space method. Description will be given first to the low-pass filter of n-th order. As the simplest example, the first order filter is exemplified.

The state equation and the output equation of $\underline{n}$-th order filter are generally expressed as below. ($\underline{n}$ is an integer)

$\dot{x}(t) = A * x(t) + B * m(t)$ (3)

$y(t) = D * y(t) + E * m(t)$ (4)

wherein

$x(t)$: state vector (column vector comprising state variables in the number of $\underline{n}$)

$\dot{x}(t)$: time derivative of state vector

A : system matrix ($\underline{n}$ lines * $\underline{n}$ columns)

$m(t)$: input-vector (column vector comprising input vectors in the number of $\underline{\ell}$)

B : control matrix ($\underline{\ell}$ lines * $\underline{n}$ columns)

$y(t)$: output-vector (column vector comprising output variables in the number of $\underline{p}$)

D : output matrix ($\underline{n}$ lines * $\underline{p}$ columns)

E : direct path matrix ($\underline{\ell}$ lines * $\underline{p}$ columns)

In the case of filters, the input-vector and the output-vector in the above equations (3) and (4) become single variables respectively. Therefore, the input-vector $m(t)$ corresponds to the input voltage $v_i(t)$ of the filter which is expressed as below.

$m(t) = V_i(t)$ (5)

The output-vector can be expressed as below because it corresponds to the output voltage $v_o(t)$ .

$y(t) = v_o(t)$ (6)

Equations (3) and (4) are expressions in time domain, and they will be expressed in $\underline{s}$ function as below if Laplace-transformed.

$sX(s) = A * X(s) + B * V_i(s)$ (7)

$V_o(s) = D * X(s) + E * V_i(s)$ (8)

wherein $X(s)$, $V_i(s)$ and $V_o(s)$ are respectively expressions of $x(t)$, $v_i(t)$ and $v_o(t)$ in $\underline{s}$-domain.

The state equations above determine the state transi tion equation when the sampling time interval is denoted T as below.
$x((k+1)T) = \Phi(T)x(kT) + \Psi(T)v_i(kT)$ (9)
$k = 0, 1, 2, 3, 4, ....$

wherein $\Phi$ and $\Psi$ in the equation (9) are obtained by
$\Phi = L^{-1}(s\epsilon - A)^{-1}$ (10)

$$\Psi = \int_0^T (T - \tau) * B\, d\tau \qquad .....(11)$$

wherein
$L^{-1}$ : inverse-Laplace transformation
$=\epsilon$ : unit matrix.
The input voltage $v_i$ which makes the output voltage of the filter arrive the final target voltage $V_b$ can be obtained as below.
$v_i(k/T = P_o^T * [\Phi(T)^{-n} * V_b - x(kT)]$ (12)
$k = 0, 1, 2, 3, 4, ....$
$P_o^T$ in the equation (12) can be obtained as a column vector forming the first line of the matrix P as below

$$R^{-1} = P = \begin{bmatrix} P_0^T \\ P_1^T \\ P_2^T \\ P_i^T \\ P_{n-1}^T \end{bmatrix}$$

$$[r_0, r_1, r_2, .....r_{n-1}] = R$$

when the matrix is defined with

$$\Phi(T) * \Psi(T) = r_0$$
$$\Phi(T) * \Psi(T) = r_1$$
$$\Phi(T) * \Psi(T) = r_2$$
$$\vdots$$
$$\Phi(T) * \Psi(T) = r_{n-1}$$

Provided $P_i^T$ is a line vector forming the i-th line of the matrix P.

In order to cause the output voltage of the filter to reach the final target voltage $V_b$ within the minimal time, the input voltage $v_i$ should be changed in accordance with the equation (12). The adding data circuit 203 in FIG. 28 calculates adding data corresponding to $v_i$ according to the equations (9) and (12). The digital adder 204 adds the adding data to the frequency controlled voltage data outputted from the ROM 201 and transmits the result to the D/A converter 6. This generates a voltage corresponding to $v_i$ in the output from the converter 6. As a result, the output voltage of the low-pass filter 202 reaches the voltage $v_b$ within the minimal time, even if the low-pass filter 202 is inserted, and the frequency switching at the VCO 4 can be conducted at high speed.

Description will now be given to the first order low-pass filter which is used as the low-pass filter shown in FIG. 28. FIG. 30 shows a first order low-pass filter comprising a resistor 221 and a capacitor 222. The transfer function G(s) indicating the relation of the input $v_i$ (s) with the output voltage vo(s) is expressed as below.

$$G(s) = V_o(s)/V_i(s) = \frac{1}{1 + s\tau} \qquad .....(13)$$

wherein $\tau$ represents time constant (CR) determinable by the resistance R of the resistor 21 and the capacitance C of the capacitor 22. As the transfer function is of the first order, the number of state variable may be one. The state variable X is assumed to be X = $V_o$. Therefore, the state equation and the output equation corresponding to the equations (7) and (8) will become as below.

$sX(s) = -(1/\tau) X(s) + (1/\tau) V_i(s)$ (14)

$V(s) = X(s)$ (15)

They are expressed in time domain as below.

$\dot{x}(t) = -(1/\tau) x(t) + (1/\tau) v_i$ (16)

$v_o(t) = x(t)$ (17)

The state transition equation is determined as below from the state equation, the output equation and the equation (9).

$x((k+1)T) = [\exp(-T/\tau)] x(kT) + [1-\exp(-T/\tau)] v_i(kT)$ (18)

$k = 0, 1, 2, 3, 4, ......$

The input voltage $v_i(kT)$ which causes the voltage to reach the target voltage $V_b$ within the minimal time is determined by the equation (12) as below.

$$v_i(kT) = \frac{\exp(-T/\tau)}{1-\exp(-T/\tau)} [[\exp(-T/\tau)] V_b - x(kT)]$$

$$k = 0, 1, 2, 3, 4, ...... \qquad .....(19)$$

Specific numerical values are substituted in the equations (18) and (19). It is assumed that the phase noise in the output of VCO 4 caused by the output noise from the D/A converter 6 is reduced by 20 dB with an offset frequency of 12.5 kHz. If a low-pass filter shown in FIG. 30 is used, the time constant $\tau$ = C * R should be ca. 0.1 msec. If the low-pass filter of the type is inserted between the D/A converter 6 and the VCO 4, the response characteristics as shown in FIG. 31a are obtained. The graph indicates the characteristics when the output voltage $V_b$ of the low-pass filter 202 is denoted as 0 [V] before switching, and the final output voltage $V_b$ after switching is denoted as 5 [V] while the vertical axis plots the error voltage coresponding to the final voltage $V_b$ of the output voltage of the low-pass filter 202. As illustrated in the graph, the prior art needs switching time of more than 1 msec as the time constant $\tau$ is set at 0.1 msec. According to the equations (18) and (19), the voltage reaches V within one sampling time (0.1 msec) if the input voltage of the low-pass filter is varied with sampling time interval T = 0.1 msec. In order to obtain the output voltage shown in FIG. 31a, the voltage shown in FIG. 31b should be supplied to the input of the low-pass filter 202.

As stated in the foregoing, response time can be shortened by temporarily applying a high voltage on the low-pass filter input immediately after switching.

FIG. 31 shows the case where the input voltage of the low-pass filter 202 is 5 [V] which reaches 8 [V] immediately after switching. The frequency switching time can further be reduced if the sampling time interval T in equations (18) and (19) is further shortened. However, if T is reduced, the voltage immediately after switching increases further, and it would often be difficult to set such a high voltage in practice. Moreover, when unsettable voltage is calculated from the equation (19), as errors are caused in $v_i$ of the equation (18), the state cannot accurately be estimated. This prolongs the response time. Therefore, when the $v_i$ obtained by the equation (19) exceeds 6 [V], the maximum voltages (saturation voltage) which is outputtable from the D/A converter 6 is assumed to be 6 [V], the value of $v_i$ in the equation (18) is substituted with 6 [V]. The response characteristic for the above is expressed in FIGs. 32a and 32b. The output from the D/A converter 6 or the input voltage of the low-pass filter 202 is limited to 6 [V] as shown in FIG. 32b, but the response time can be limited within 2 sampling times or less (2 msec) as shown in FIG. 32a.

FIG. 33 is a block diagram to show the second embodiment of VCO control circuit wherein the output data of the ROM 201 is converted from digital to analog by the D/A converter 6 and the output voltage therefrom is inputted at the analog adder 206. The output voltage of the adder voltage generating circuit 205 is supplied to the other input of the analog adder 206. The circuit 205 outputs adding voltage when the

desired frequency data is inputted. The effect similar to that of the first embodiment can be obtained with the above construction.

Frequency can be switched at a high speed even if a low-pass filter is inserted in order to suppress the noises in the output from the D/A converter. Accordingly, by incorporating such VCO control circuits within the control circuits shown in FIGs. 15 and 16, a frequency synthesizer which has low noises and which can be switched in frequency at high speed can be realized.

FIGs. 34 and 35 show frequency switching characteristics when the oscillation frequency is switched from 1440 GHz to 1465 Ghz. The reference frequency is assumed to be 6.25 kHz. FIG. 34 shows the characteristics obtained by the conventional frequensy synthesizer FIG. 1 while FIG. 35 indicates the characteristics obtained by the embodiment of this invention shown in FIG. 10. While frequency varies across 250 msec after frequency switching in the prior art system, almost no frequency variation occurs in the embodiment of this invention to enable high speed frequency switching less than 1 msec.

## Claims

1. A frequency synthesizer of the type comprising a voltage controlled oscillator, a variable ratio divider which divides the output from said voltage controlled oscillator, a phase detector which compares the output phase of said variable ratio divider with the output of a reference signal, a loop filter which smoothens the output from said phase detector and supplies the same to said voltage controlled oscillator, and an oscillation frequency switching means which switches the oscillation frequency of said voltage controlled oscillator by changing the division ratio of said variable ratio divider wherein said oscillation frequency switching means includes a voltage supply means which supplies a steering voltage corresponding to the oscillation frequency after switching to said voltage controlled oscillator via a D/a converter in synchronization with the change of division ratio at said variable ratio divider, which is characterized in that said voltage controlled oscillator is an oscillator which changes oscillation frequency corresponding to a steering voltage non-linearly, a voltage measuring means is provided which measures the voltage supplied from said loop filter to said voltage controlled oscillator via an A/D converter before switching of the oscillation frequency, and said voltagep supply means includes a steering voltage compensation means which corrects said steering voltage which is to be supplied to said voltage controlled oscillator based on the measured value by said voltage measuring means correspondingly to the non-linearity of the voltage controlled oscillator.

2. The frequency synthesizer as claimed in Claim 1 wherein the steering voltage compensation means includes a means which adds the output from said loop filter to a voltage which is expressed by the formula below:

$V_{s2} - (\Delta V_{s2} - \Delta V_{s1})$

wherein the value obtained by the voltage measuring means is represented with $-\Delta V_{s1}$, the frequency drifts of said voltage controlled oscillator caused by the voltage $-\Delta V_{s1}$ with $\Delta f_o$, the steering voltage corresponding to the oscillation frequency after switching with $V_{s2}$, and the voltage necessary to shift the oscillation frequency of said voltage controlled oscillator $\Delta f_o$ after switching of oscillation frequency with $-\Delta V_{s2}$.

3. The frequency synthesizer as claimed in claim 1 wherein a sample hold circuit is connected to an output of the D/A converter, and a means is provided for stopping the power supply to said D/A converter after a steering voltage is held at the sample hold circuit.

4. The frequency synthesizer as claimed in Claim 3 wherein the sample hold circuit includes a capacitor, and the capacitor is the same as the capacitor which is an element of the loop filter.

5. The frequency synthesizer as claimed in Claim 1 wherein a variable bandwidth filter is connected to an output of the D/A converter, and the oscillation frequency switching means includes a bandwidth limiting means which narrows the bandwidth of said variable bandwidth filter after switching the oscillation frequency.

6. The frequency synthesizer as claimed in Claim 1 wherein a variable bandwidth filter is connected to an input of the voltage controlled oscillator, and the oscillation frequency switching means includes a bandwidth limiting means which narrows the bandwidth of said variable bandwidth filter after switching of the oscillation frequency.

7. The frequency synthesizer as claimed in Claim 1 wherein a low-pass filter is connected to an output of the D/A converter, and the voltage supply means includes a means which sequentially sets plural different voltages before setting steering voltage at the D/A converter output correspondingly to the frequency after switching.

8. A frequency synthesizer comprising a voltage controlled oscillator, a variable ratio divider which divides the output from said voltage controlled oscillator, a phase detector which compares the output

phase of said variable ratio divider with the phase of a reference signal, a loop filter which smoothens the output of the phase detector and supplies it to said voltage controlled oscillator, and an oscillation frequency switching means which switches oscil lation frequency of said voltage controlled oscillator by changing the division ratio of said variable ratio divider wherein said frequency oscillation switching means includes a voltage supply means which supplies a steering voltage corresponding to the oscillation frequency after switching to said voltage controlled oscillator via a D/A converter in synchronization with the change of division ratio of said variable ratio divider, which is characterized in that said variable ratio divider is a variable ratio divider, with a reset means, and the oscillation frequency switching means includes a means which resets said variable ratio divider by using the reference signal inputted in the phase detector as a trigger.

9. The frequency synthesizer as Claimed in Claim 8 wherein a loop switch is provided at an input of the loop filter, and the oscillation frequency switching means includes a switch ON/OFF means which opens said loop switch before switching the oscillation frequency and closes said loop switch after the variable ratio divider is reset.

10. The frequency synthesizer as claimed in Claim 8 wherein the voltage controlled oscillator is an oscillator where oscillation frequency corresponding to the input steering voltage changes non-linearly, a voltage measuring means is provided which measures via an A/D converter the voltage supplied from the loop filter to the voltage controlled oscillator before switching of the oscillation frequency, and the voltage supply means includes a steering voltage compensation means which corrects the steering voltage supplied to said voltage controlled oscillator correspondingly to the non-linearity of the voltage controlled oscillator based on the measured value by said voltage measuring means.

11. The frequency synthesizer as claimed in Claim 8 wherein a sample hold circuit is connected to an output of the D/A converter, and the synthesizer is provided with a means which stops the power supply to said D/A converter after a steering voltage is held at the sample hold circuit.

12. The frequency synthesizer as claimed in Claim 11 wherein the sample hold circuit includes a capacitor, and the capacitor is the same capacitor which is a component element of the loop filter.

13. The frequency synthesizer as claimed in Claim 8 wherein a variable bandwidth filter is connected to an output of the D/A converter, and the oscillation frequency switching means includes a bandwidth limiting means which narrows the bandwidth of said variable bandwidth filter after switching of the oscillation frequency.

14. The frequency synthesizer as claimed in Claim 8 wherein a variable bandwidth filter is connected to an input of the voltage controlled oscillator, and the oscillation frequency switching means includes a bandwidth limiting means which narrows the bandwidth of said variable bandwidth filter after switching of oscillation frequency.

15. The frequency synthesizer as claimed in Claim 8 wherein a low-pass filter is connected to an output of the D/A converter, and the voltage supply means includes a means which sequentially sets plural different voltages at frequency switching before setting a steering voltage corresponding to the frequency after switching at the D/A converter.

16. A frequency synthesizer, for providing oscillations at selected frequencies over a frequency range, including a voltage controlled oscillator (VCO) belonging to a phase-locked loop (PLL) system that has a divider circuit for setting the VCO operating frequency, and a control circuit, connected to the PLL system, capable of setting the operating frequency of the frequency synthesizer by setting both the division ratio of the divider circuit and a voltage for controlling the VCO, and in which the control circuit includes means for compensating for a non-linear relationship between the VCO frequency and its control voltage in setting the voltage for controlling the VCO.

17. A frequency synthesizer as claimed in claim 16, wherein the control circuit includes means for sensing a control voltage, provided by the PLL system, for maintaining the VCO at its set frequency, and including means responsive to the sensed control voltage to provide a new control voltage for the VCO, when setting the frequency synthesizer to a new operating frequency, that causes the frequency synthesizer to operate at the new frequency with substantially no change in the sensed control voltage.

18. A method of generating oscillations at selected frequencies over a frequency range, by means of a frequency synthesizer that includes a voltage-controlled oscillator (VCO) belonging to a phase-locked loop (PLL) system that has a divider circuit for setting the VCO frequency, including the step of seetting the operating frequency of the synthesizer by setting both the division ratio of the divider circuit and a voltage for controlling the VCO, where the control voltage provided by the control circuit compensates for a non-linear relationship between the VCO frequency and its control voltage.

19. A method of generating oscillations at selected frequencies over a frequency range as claimed in claim 18, including the steps of sensing a control voltage, provided by the PLL, for maintaining the VCO at

its set frequency, and of using the sensed control voltage, in providing a new control voltage for the VCO, when setting the frequency synthesizer to a new operating frequency, to cause operation of the frequency synthesizer at the new frequency with substantially no change in the sensed control voltage.

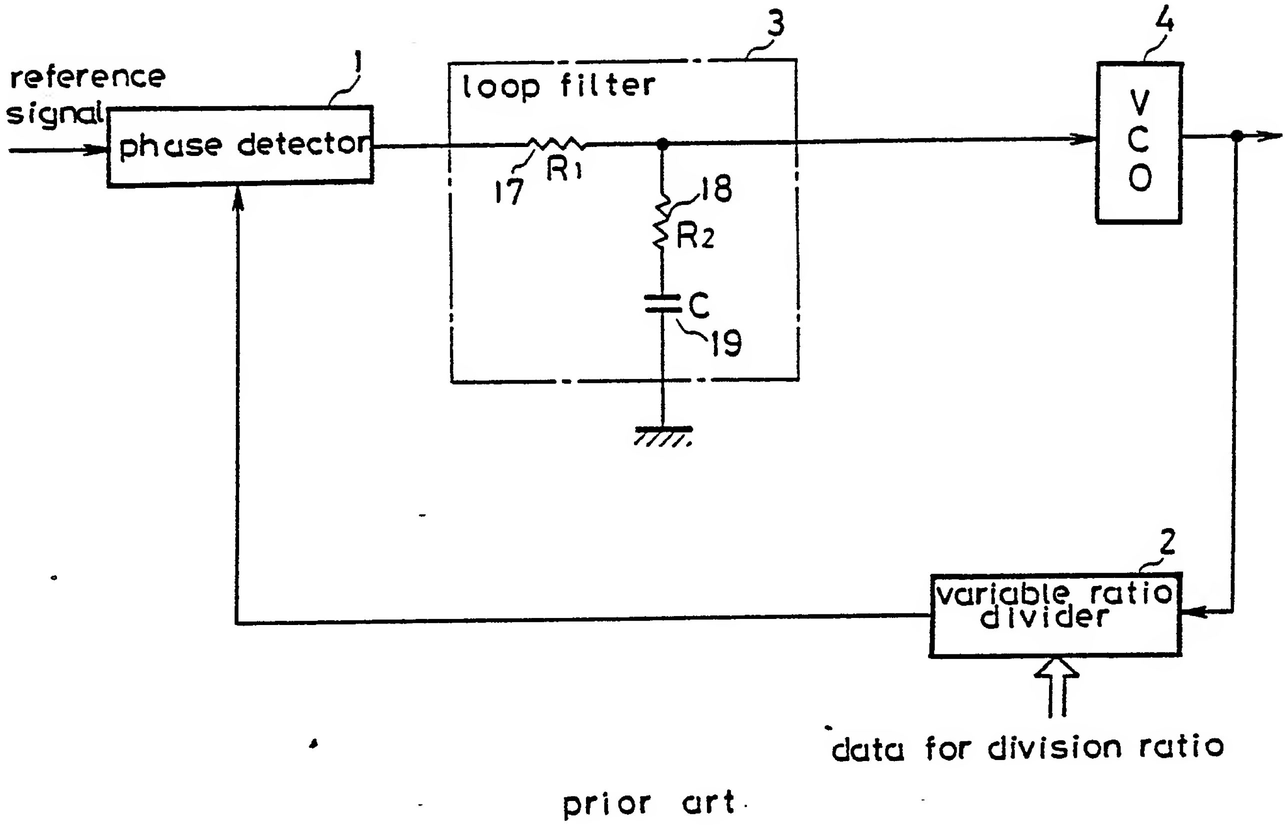

reference signal
phase detector
1
loop filter
3
17
R1
18
R2
C
19
VCO
4
variable ratio divider
2
data for division ratio
prior art

FIG. 1

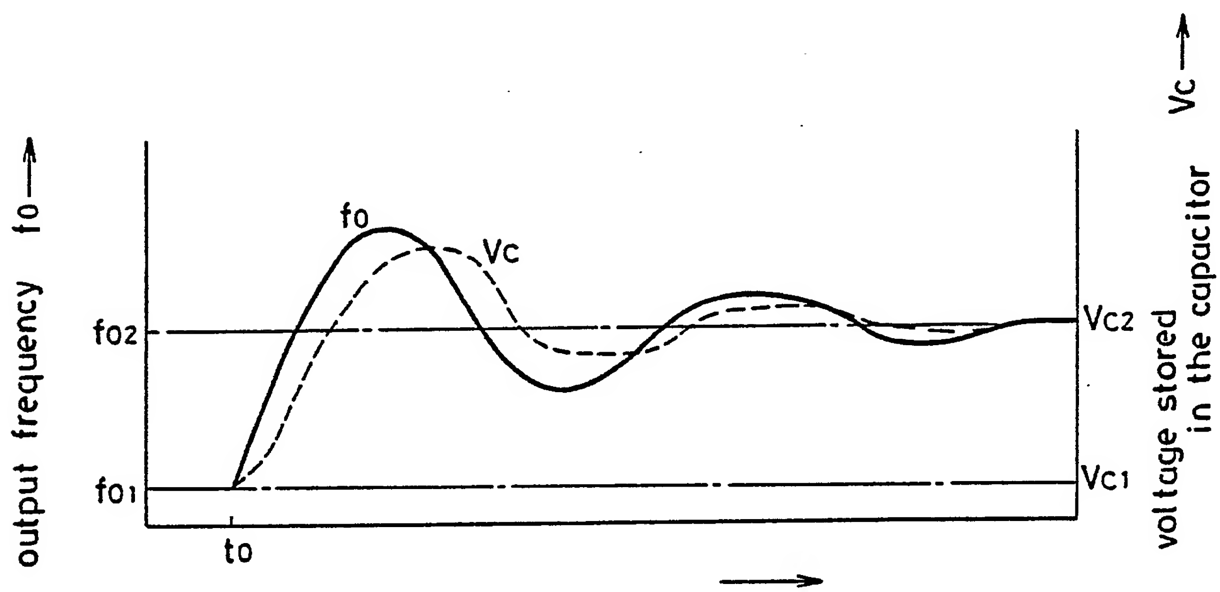
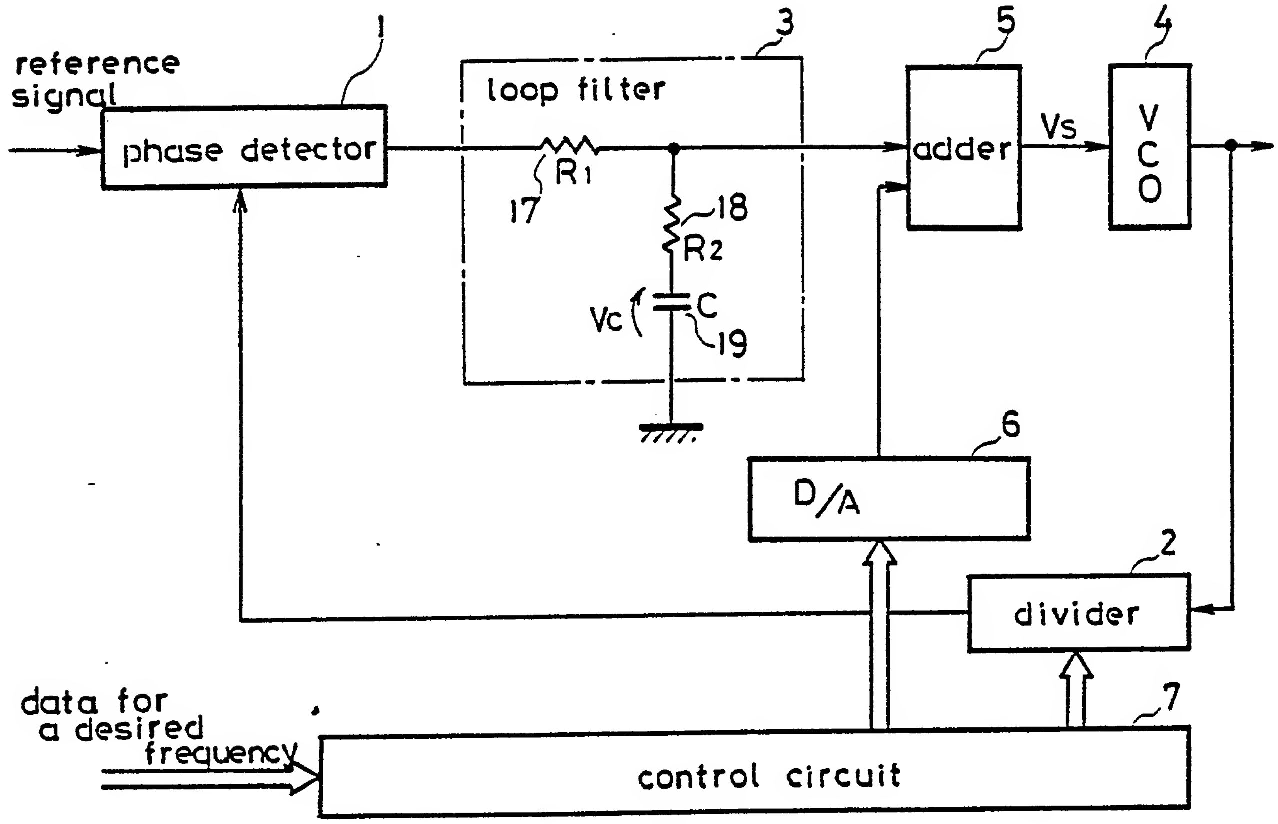

output frequency fo
fo
Vc
fo2
fo1
to
Vc2
Vc1
voltage stored in the capacitor
Vc

FIG. 2




prior art

FIG. 3

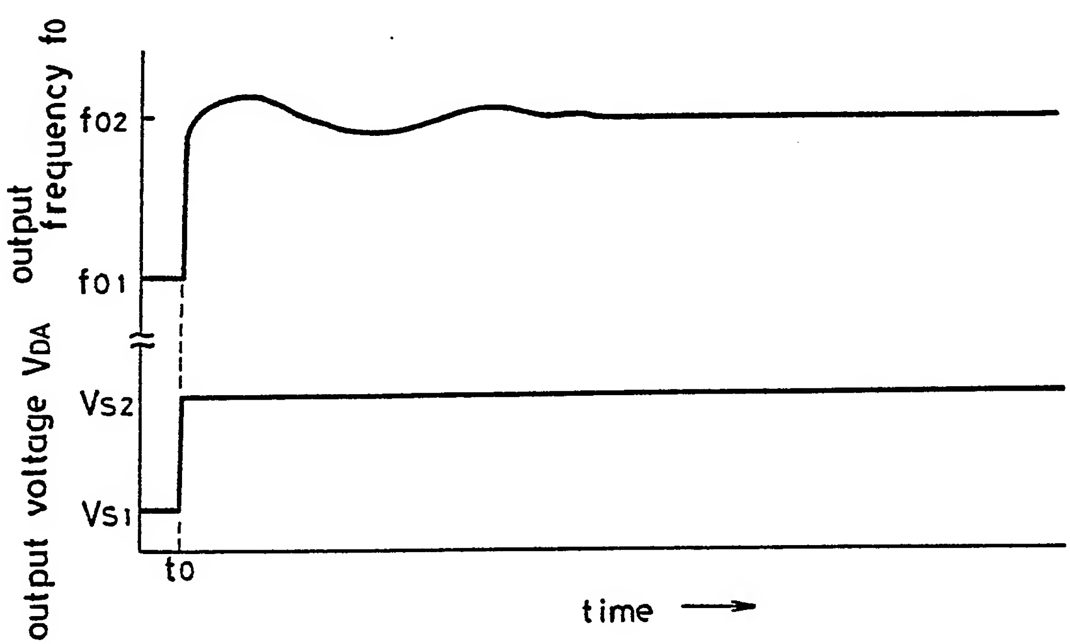
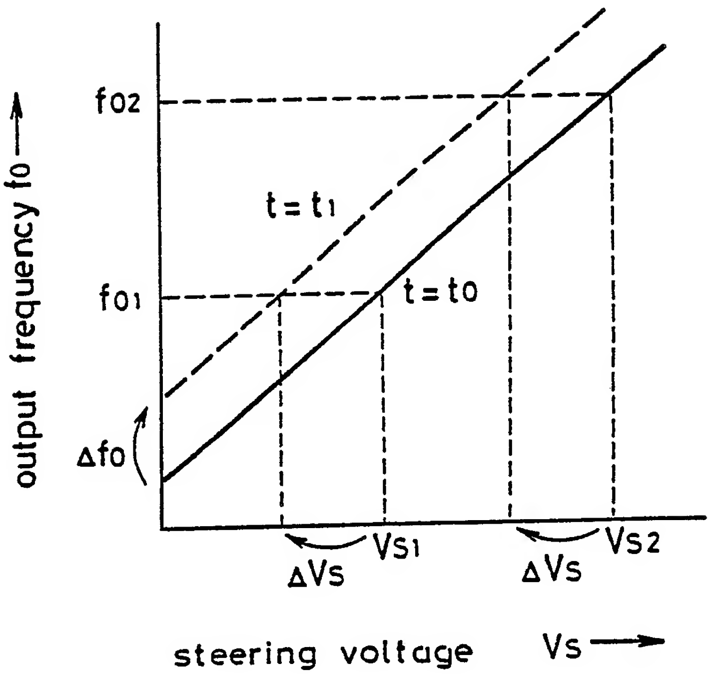
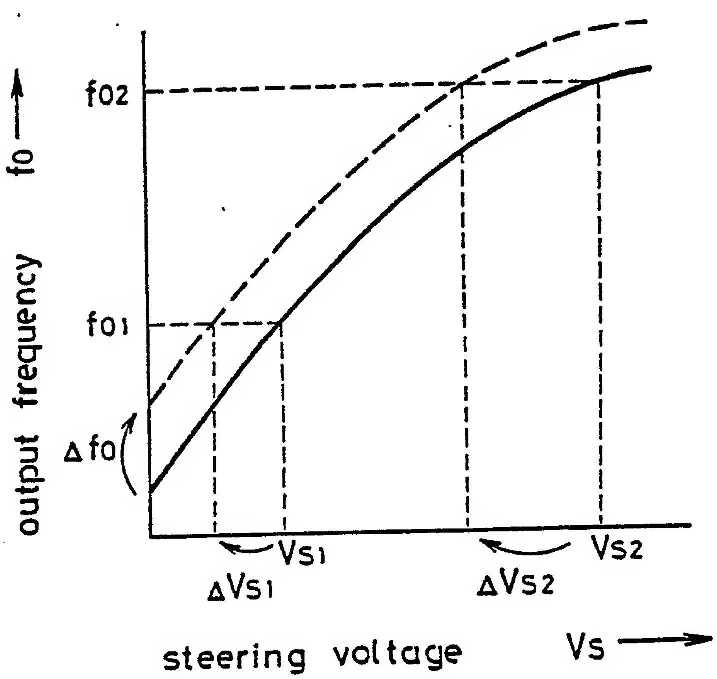



FIG. 4



output frequency fo
fo2
fo1
t = t1
t = t0
Δfo
Vs1
ΔVs
Vs2
ΔVs
steering voltage
Vs


FIG. 5



output frequency fo
fo2
fo1
Δfo
Vs1
ΔVs1
Vs2
ΔVs2
steering voltage
Vs


FIG. 6

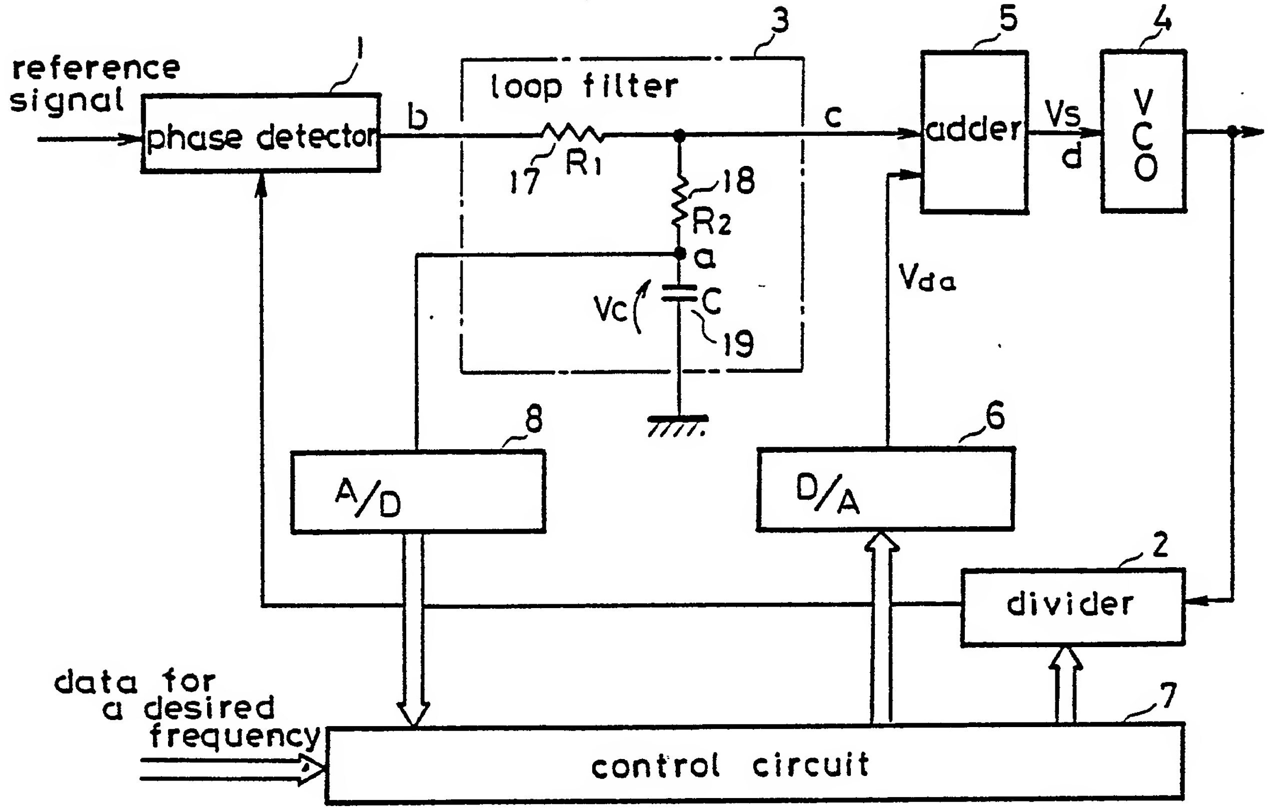

reference signal
phase detector
1
b
loop filter
3
R1
17
18
R2
a
Vc
C
19
c
adder
5
Vs
d
VCO
4
Vda
A/D
8
D/A
6
divider
2
data for a desired frequency
control circuit
7

FIG. 7

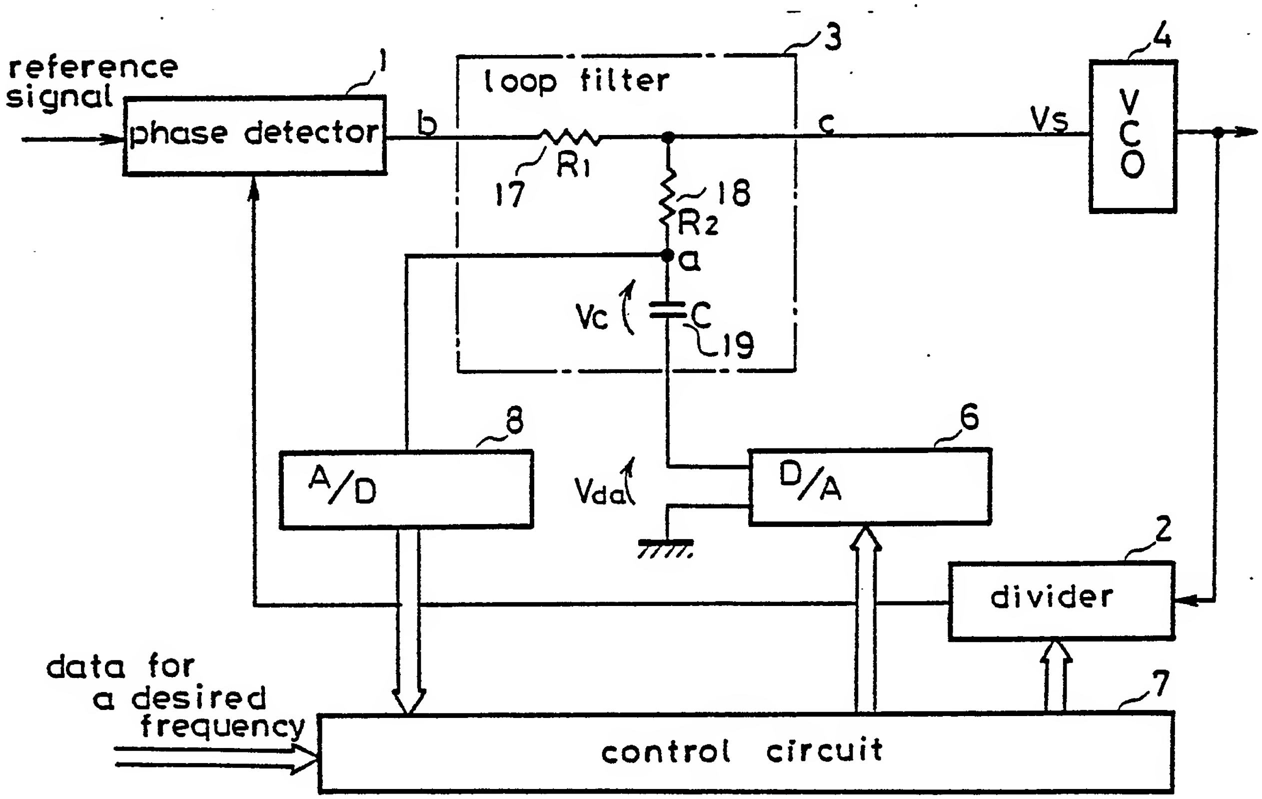

reference signal
phase detector
1
b
loop filter
3
R1
17
18
R2
a
Vc
C
19
c
Vs
VCO
4
A/D
8
Vda
D/A
6
divider
2
data for a desired frequency
control circuit
7

FIG. 8

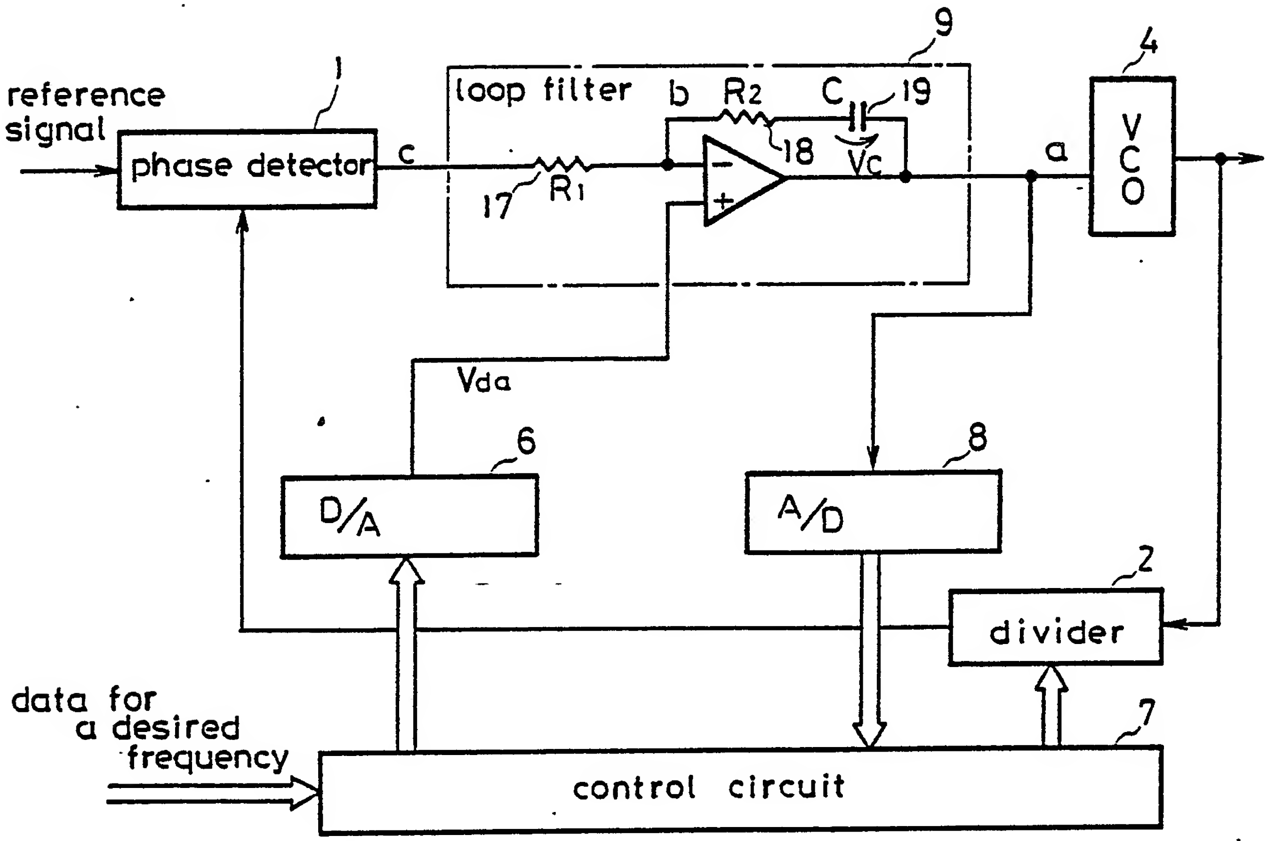

reference signal
phase detector
1
c
loop filter
9
b
R2
C
19
18
Vc
17
R1
a
4
VCO
Vda
6
D/A
8
A/D
2
divider
data for a desired frequency
7
control circuit

FIG. 9

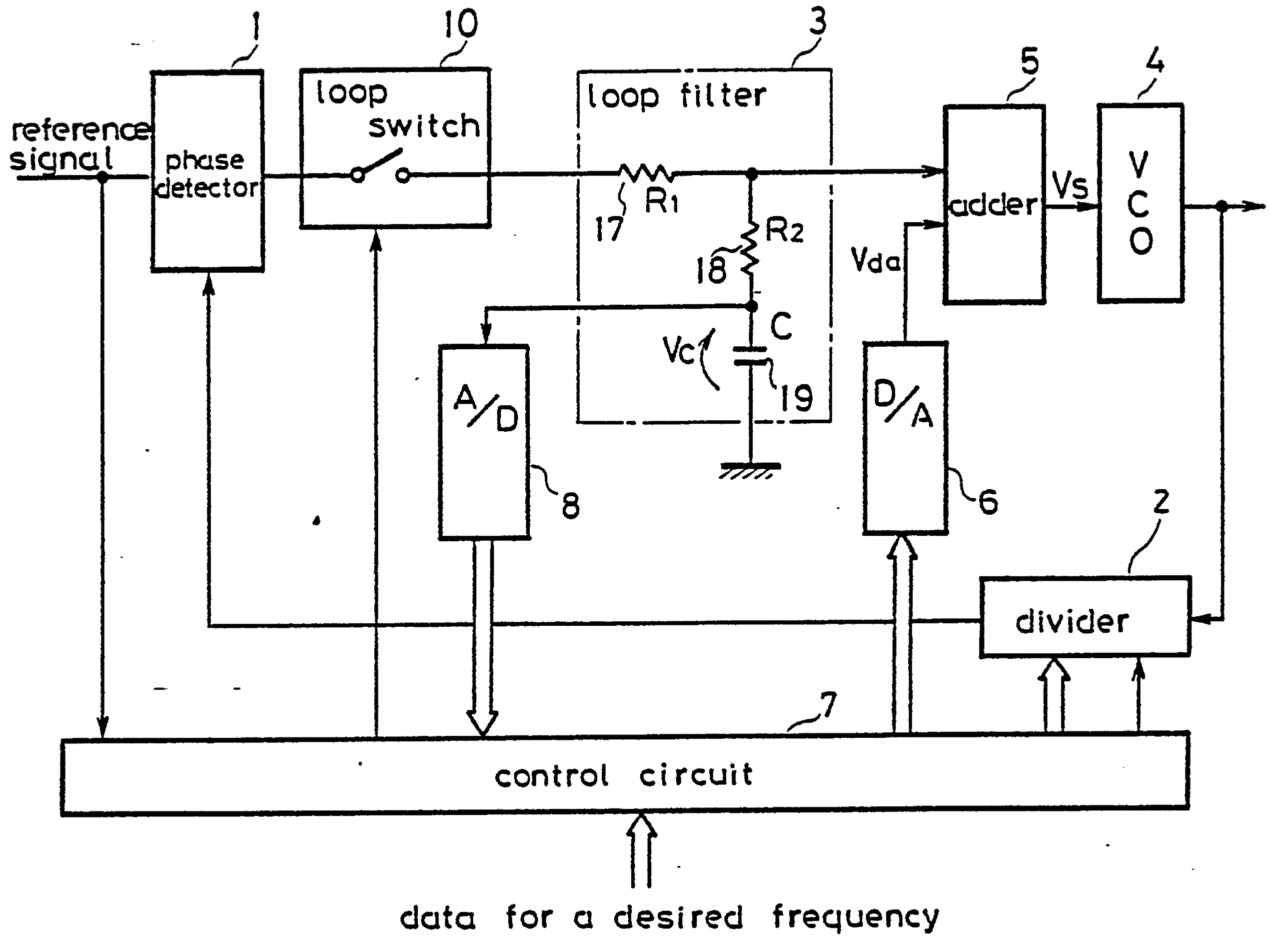

reference signal
phase detector
loop switch
loop filter
adder
V C O
Vs
R1
R2
C
Vc
Vda
A/D
D/A
divider
control circuit
data for a desired frequency
1
10
3
5
4
17
18
19
8
6
2
7

FIG. 10

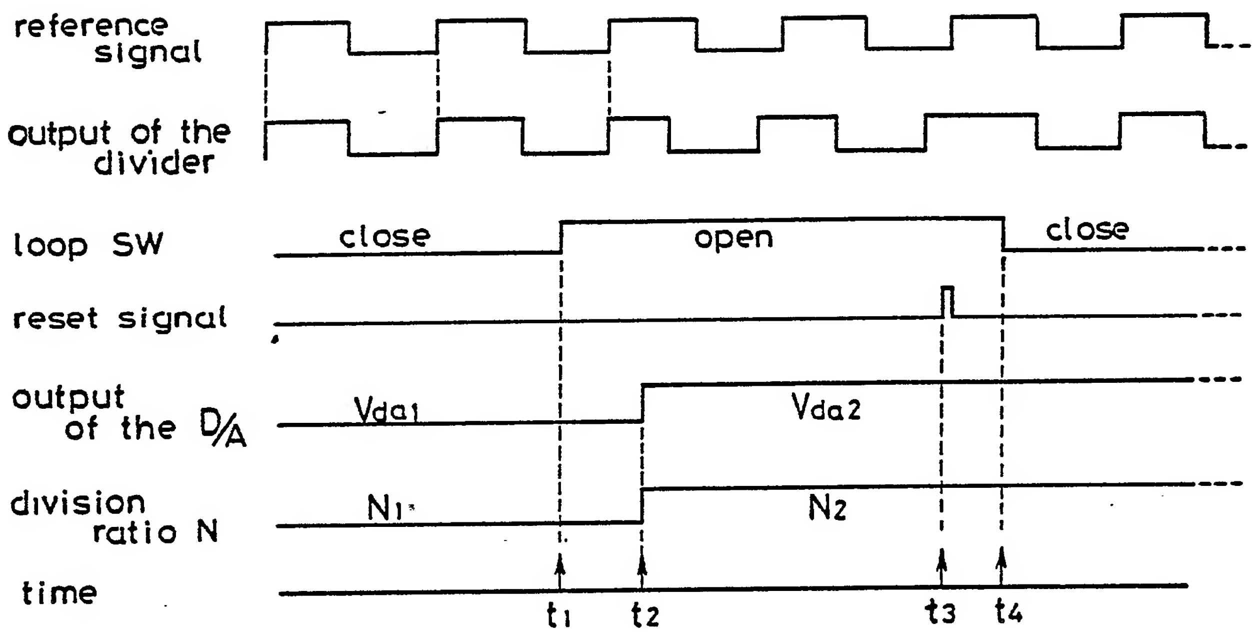

reference signal
output of the divider
loop SW
close
open
close
reset signal
output of the D/A
Vda1
Vda2
division ratio N
N1
N2
time
t1
t2
t3
t4

FIG. 11

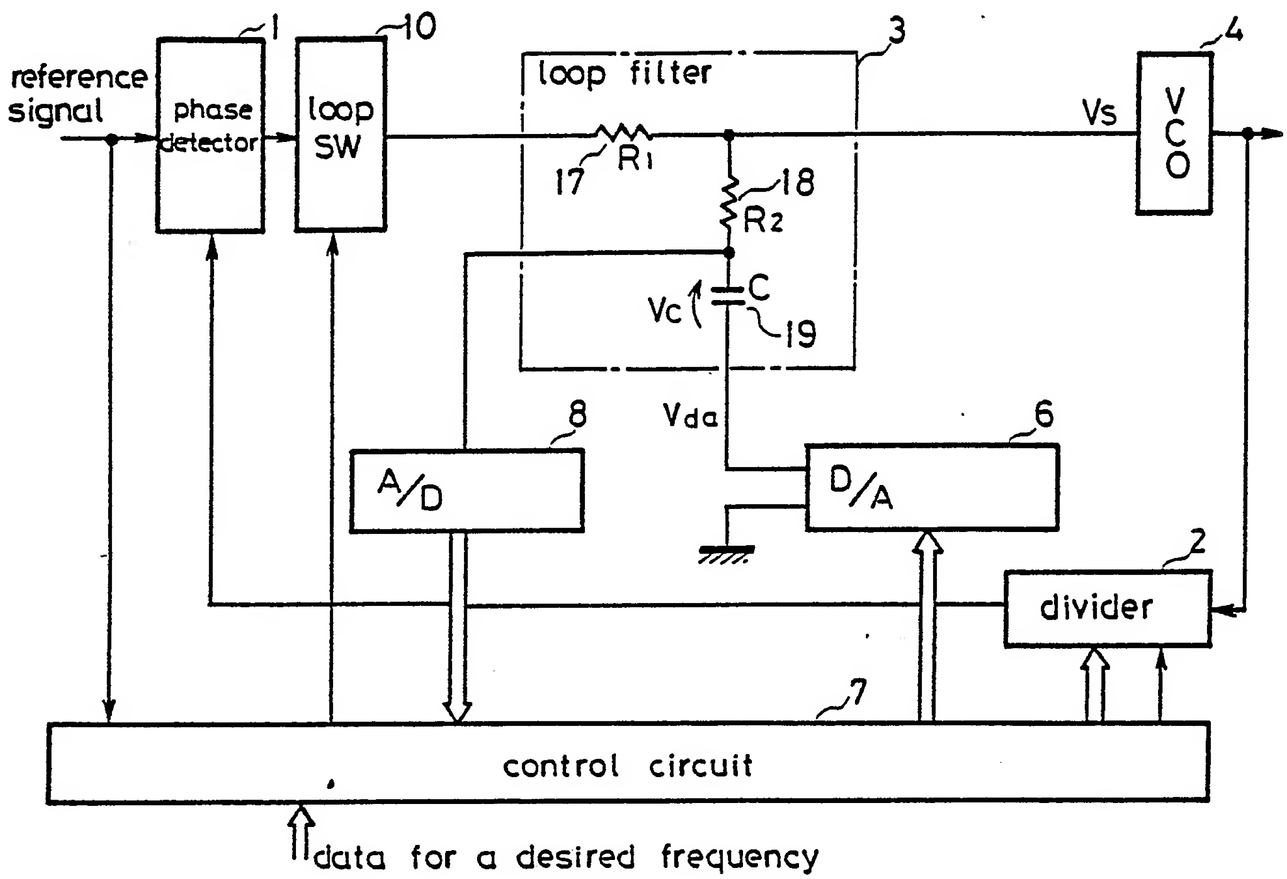

reference signal
phase detector
loop SW
loop filter
Vs
VCO
R1
17
18
R2
C
Vc
19
Vda
8
A/D
6
D/A
2
divider
7
control circuit
data for a desired frequency
1
10
3
4

FIG. 12

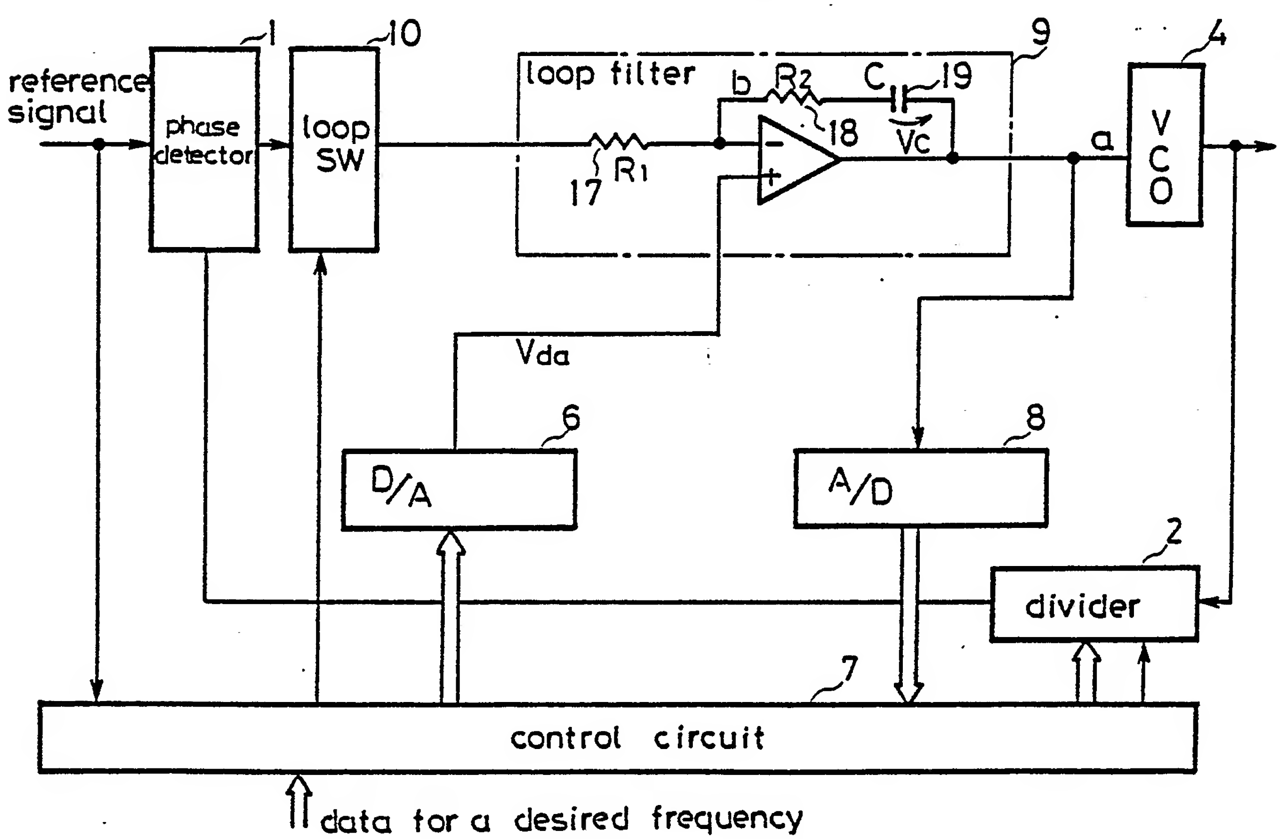

reference signal
phase detector
loop SW
loop filter
b
R2
C
19
18
Vc
a
VCO
R1
17
Vda
6
D/A
8
A/D
2
divider
7
control circuit
data for a desired frequency
1
10
9
4

FIG. 13

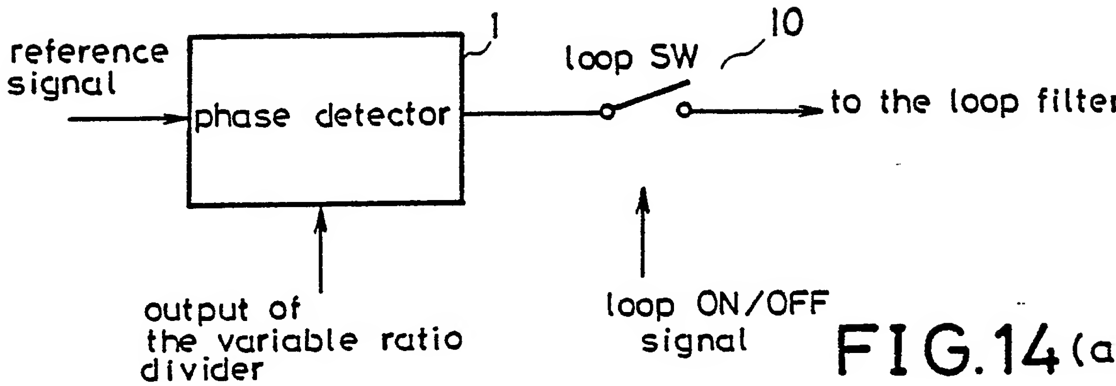



FIG.14(a)

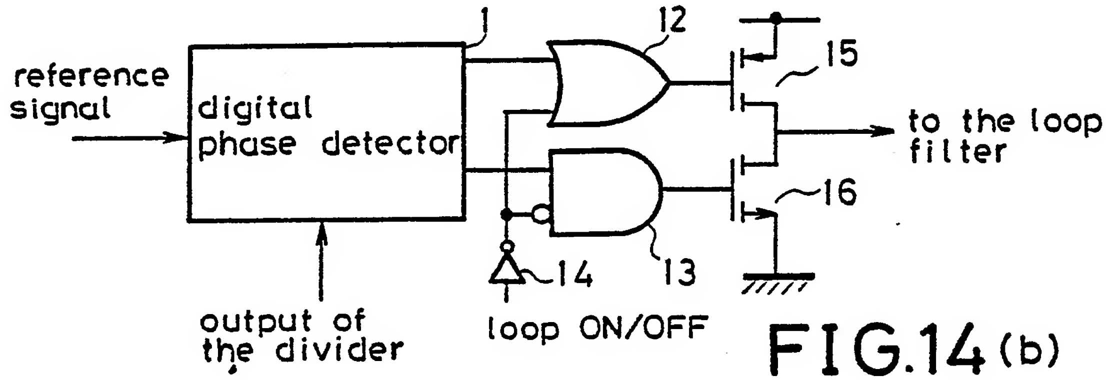



FIG.14(b)

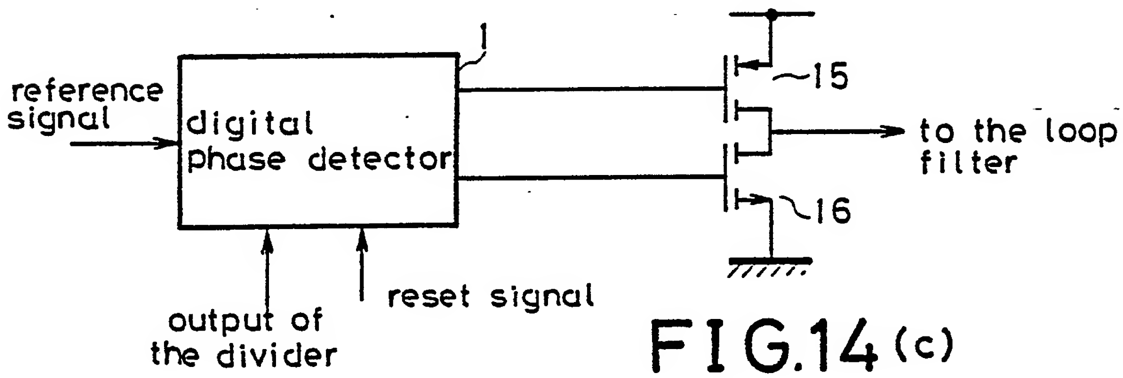



FIG.14(c)

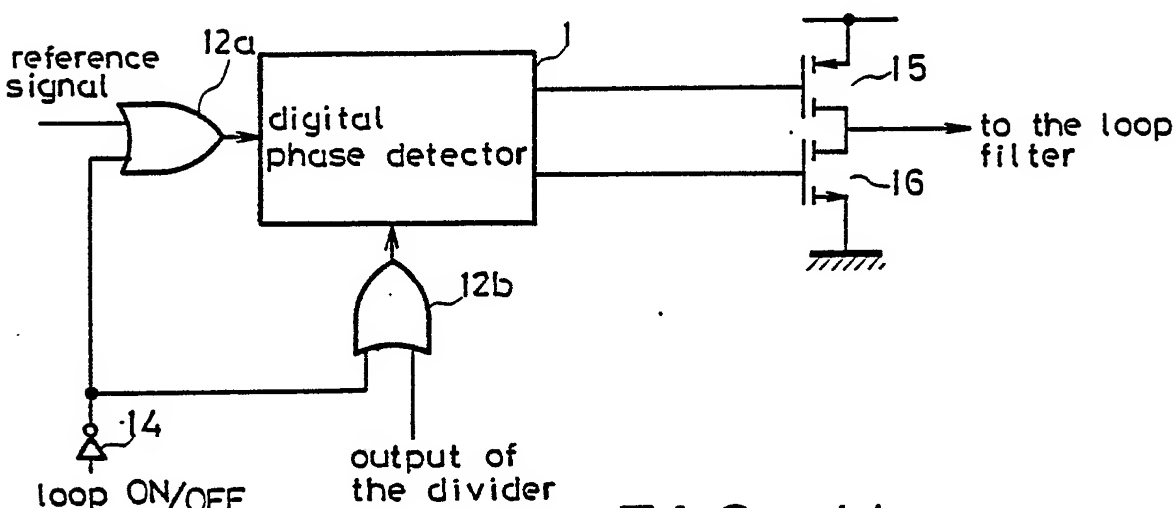



FIG. 14(d)

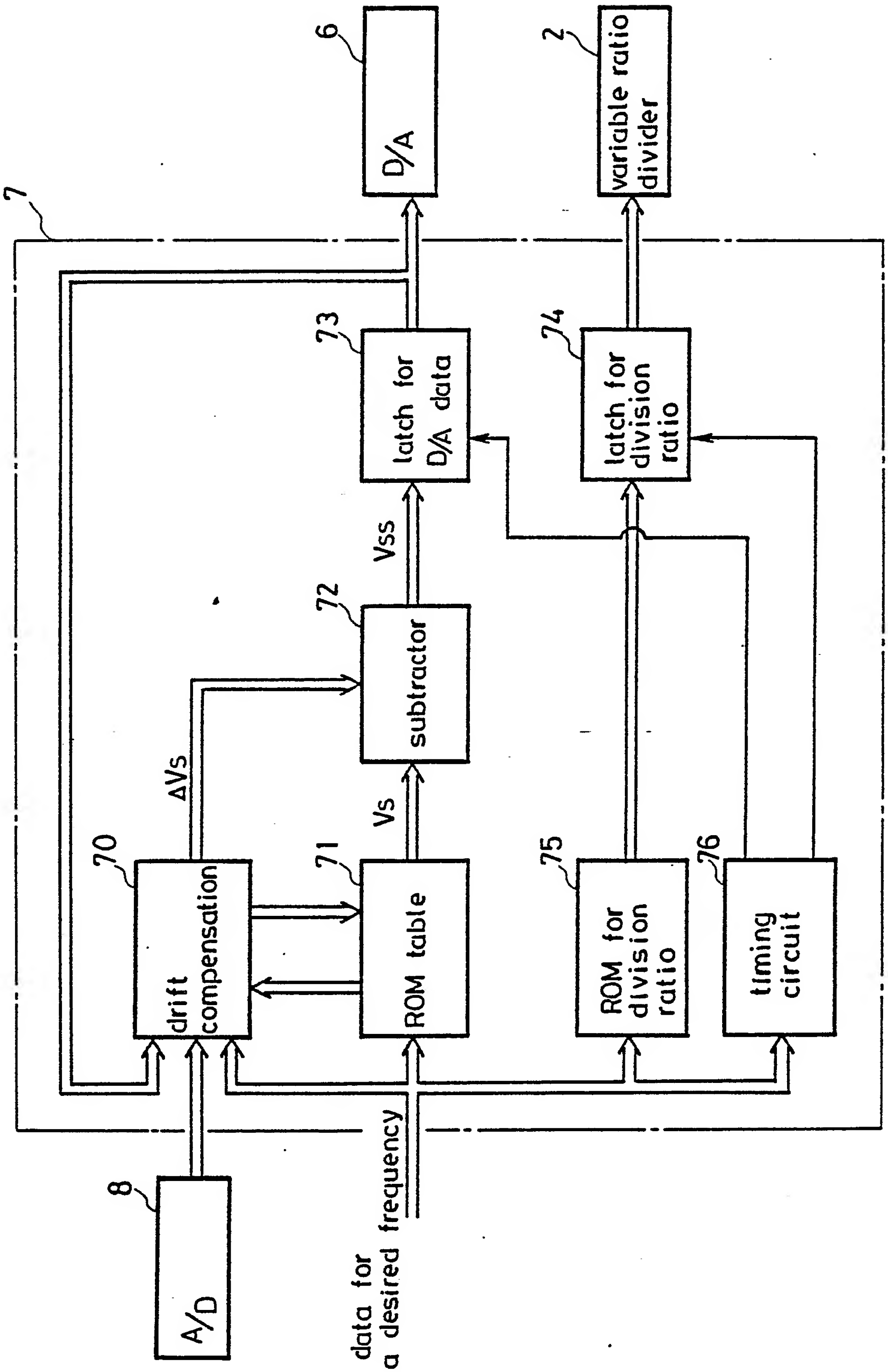

6
D/A
2
variable ratio divider
7
73
latch for D/A data
74
latch for division ratio
Vss
72
subtractor
ΔVs
Vs
70
drift compensation
71
ROM table
75
ROM for division ratio
76
timing circuit
8
A/D
data for a desired frequency

FIG. 15

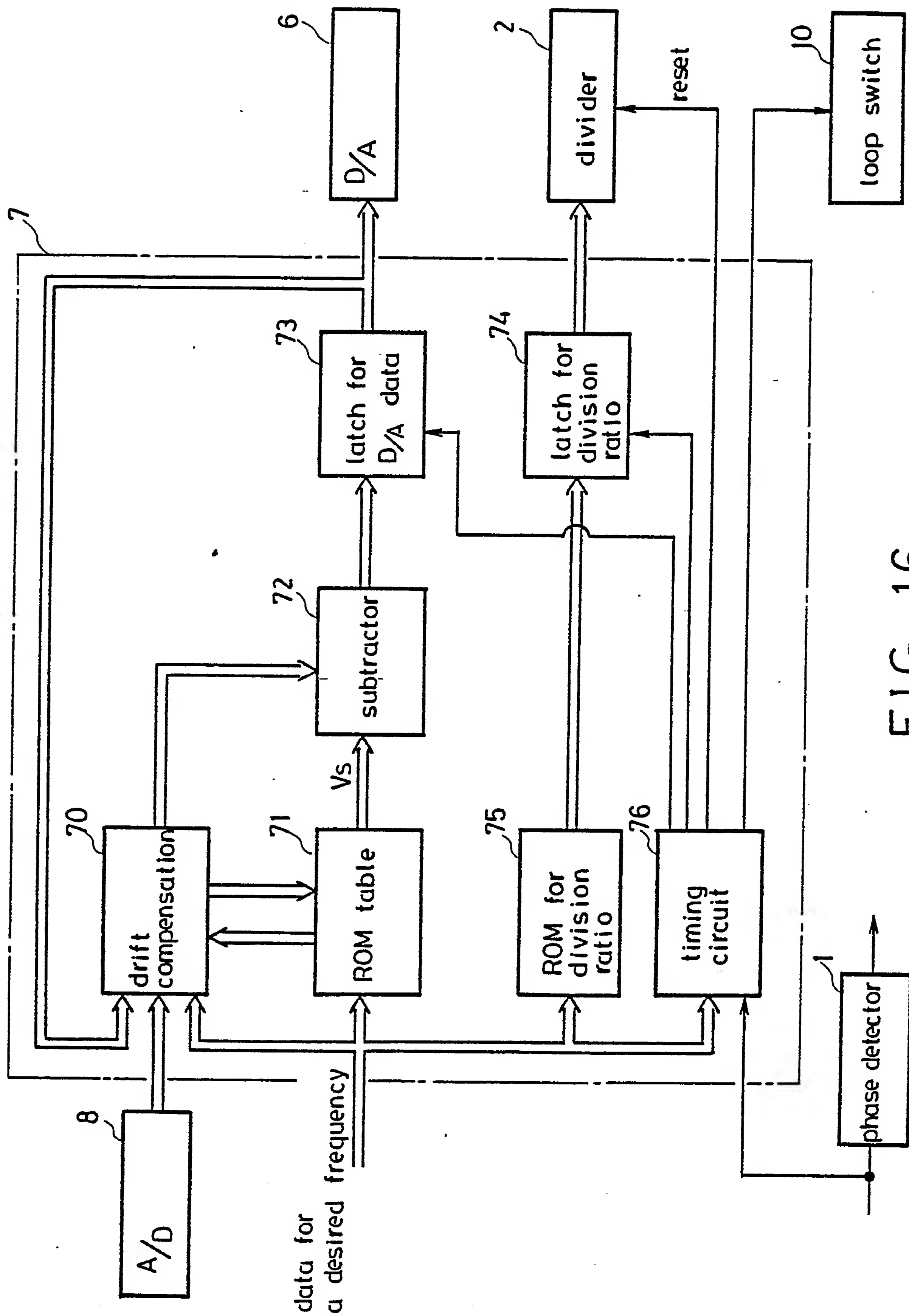

A/D
8
data for
a desired frequency
drift
compensation
70
ROM table
71
Vs
subtractor
72
latch for
D/A data
73
D/A
6
ROM for
division
ratio
75
timing
circuit
76
latch for
division
ratio
74
divider
2
reset
loop switch
10
phase detector
1
7

FIG. 16

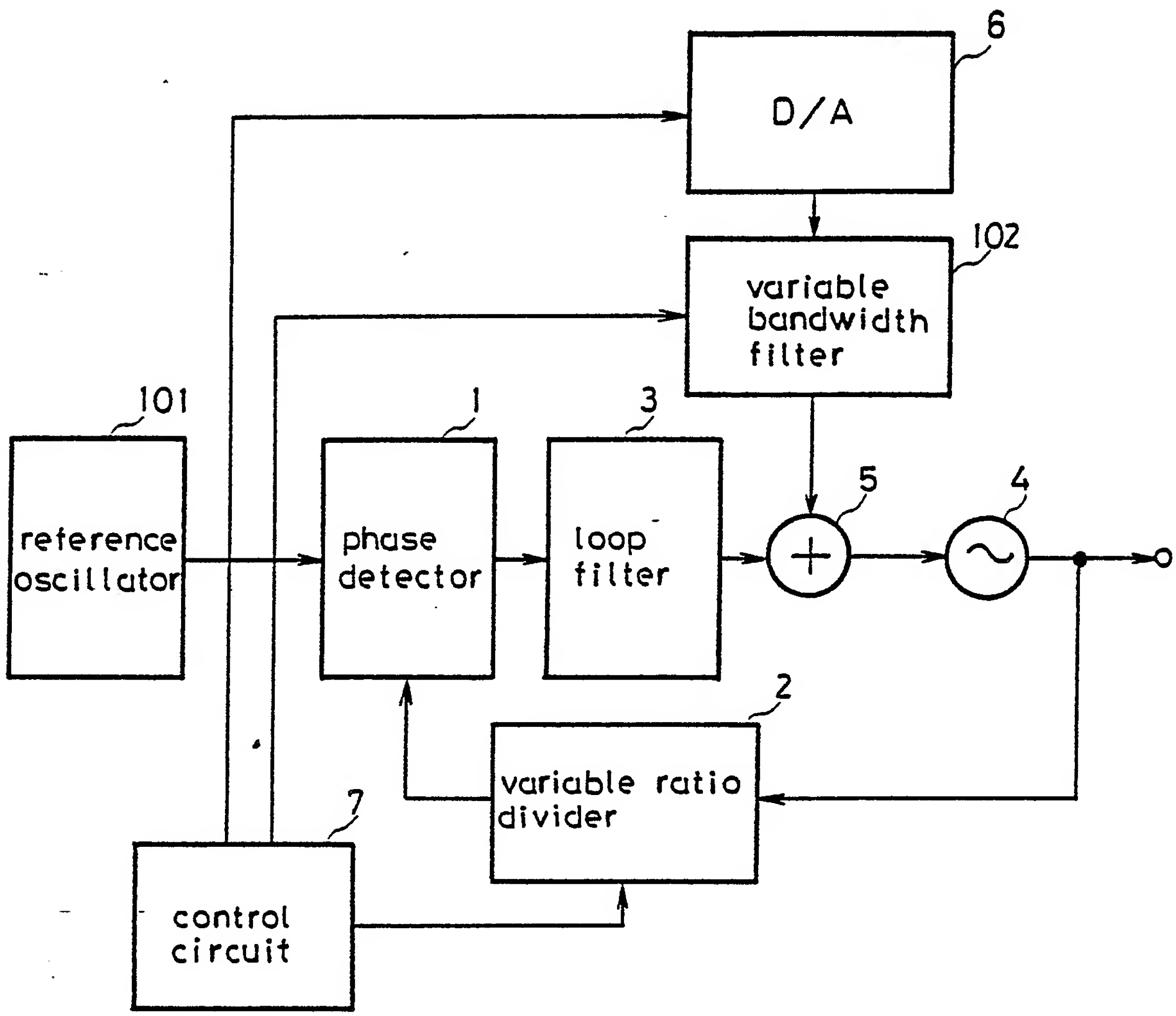



FIG. 17

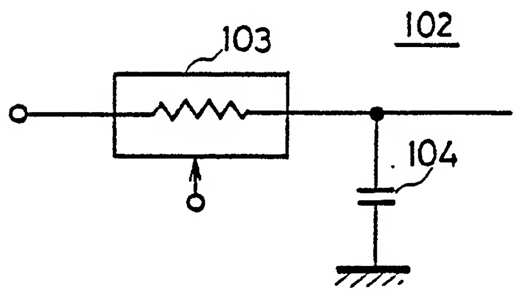



FIG. 18

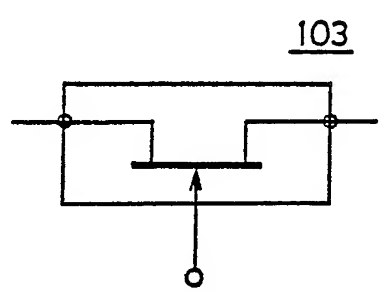



FIG. 19

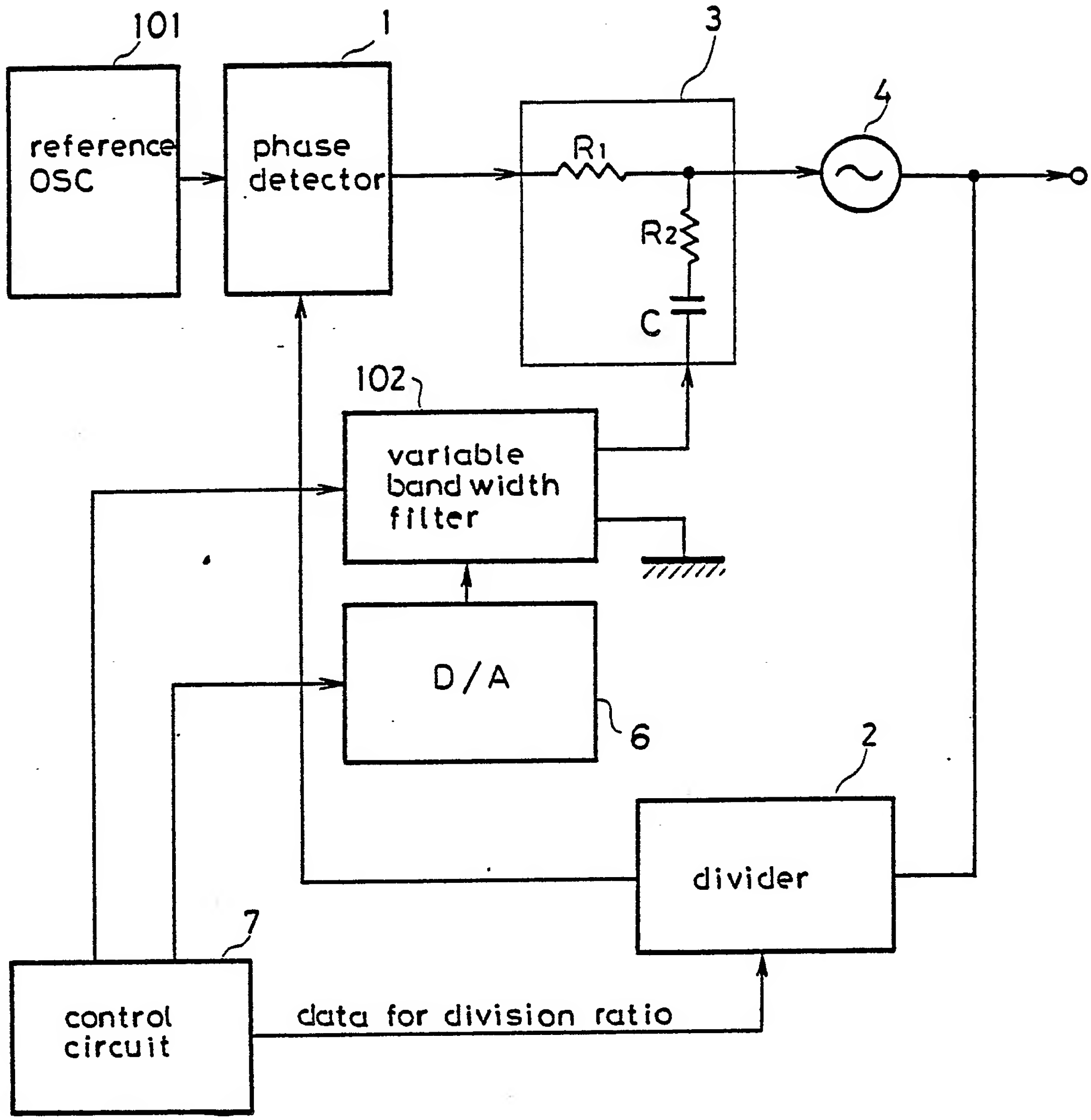

101
reference OSC
1
phase detector
3
R1
R2
C
4
102
variable band width filter
D/A
6
2
divider
7
control circuit
data for division ratio

FIG. 20

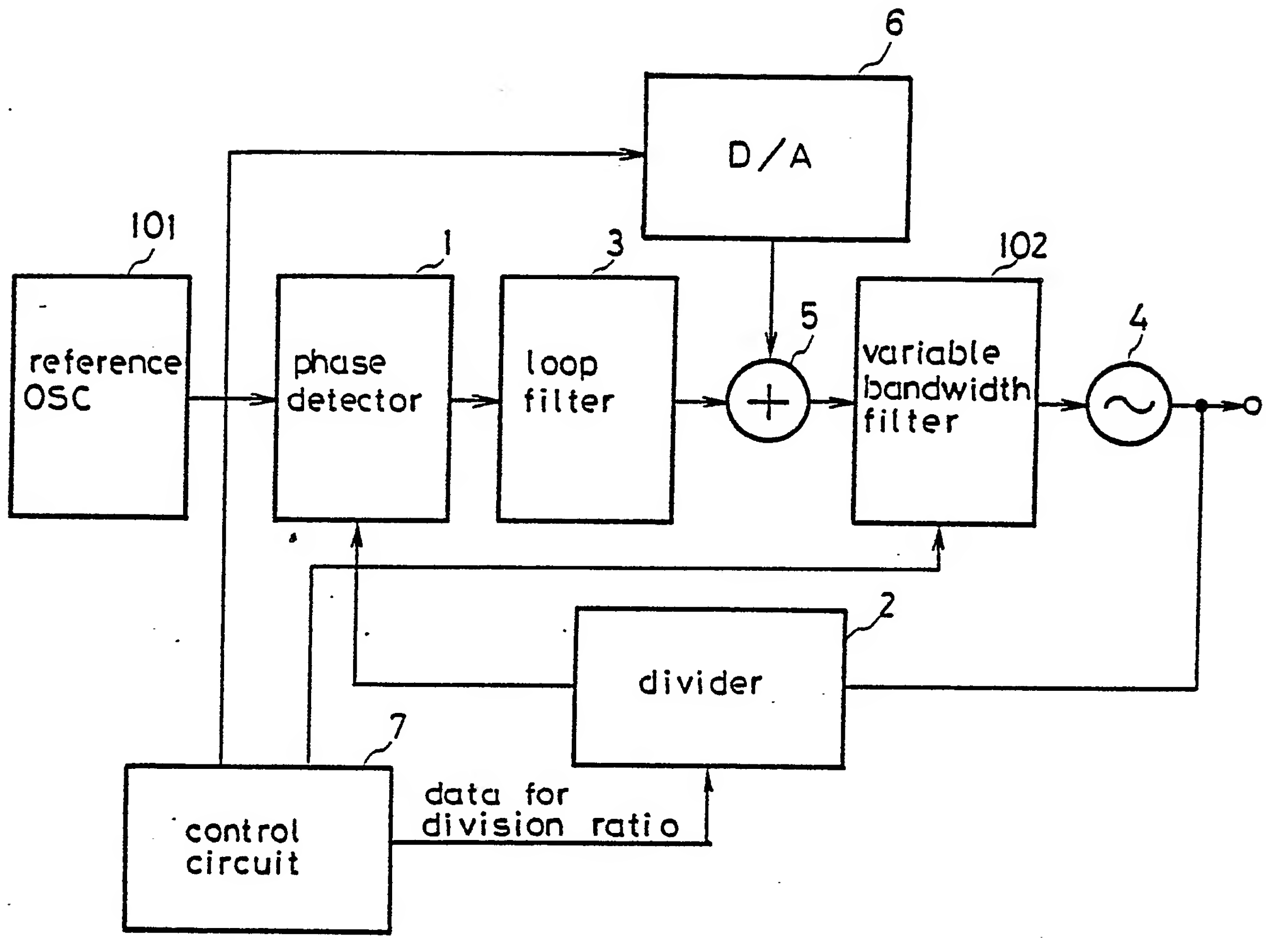

6
D/A
101
reference OSC
1
phase detector
3
loop filter
5
102
variable bandwidth filter
4
2
divider
7
control circuit
data for division ratio

FIG. 21

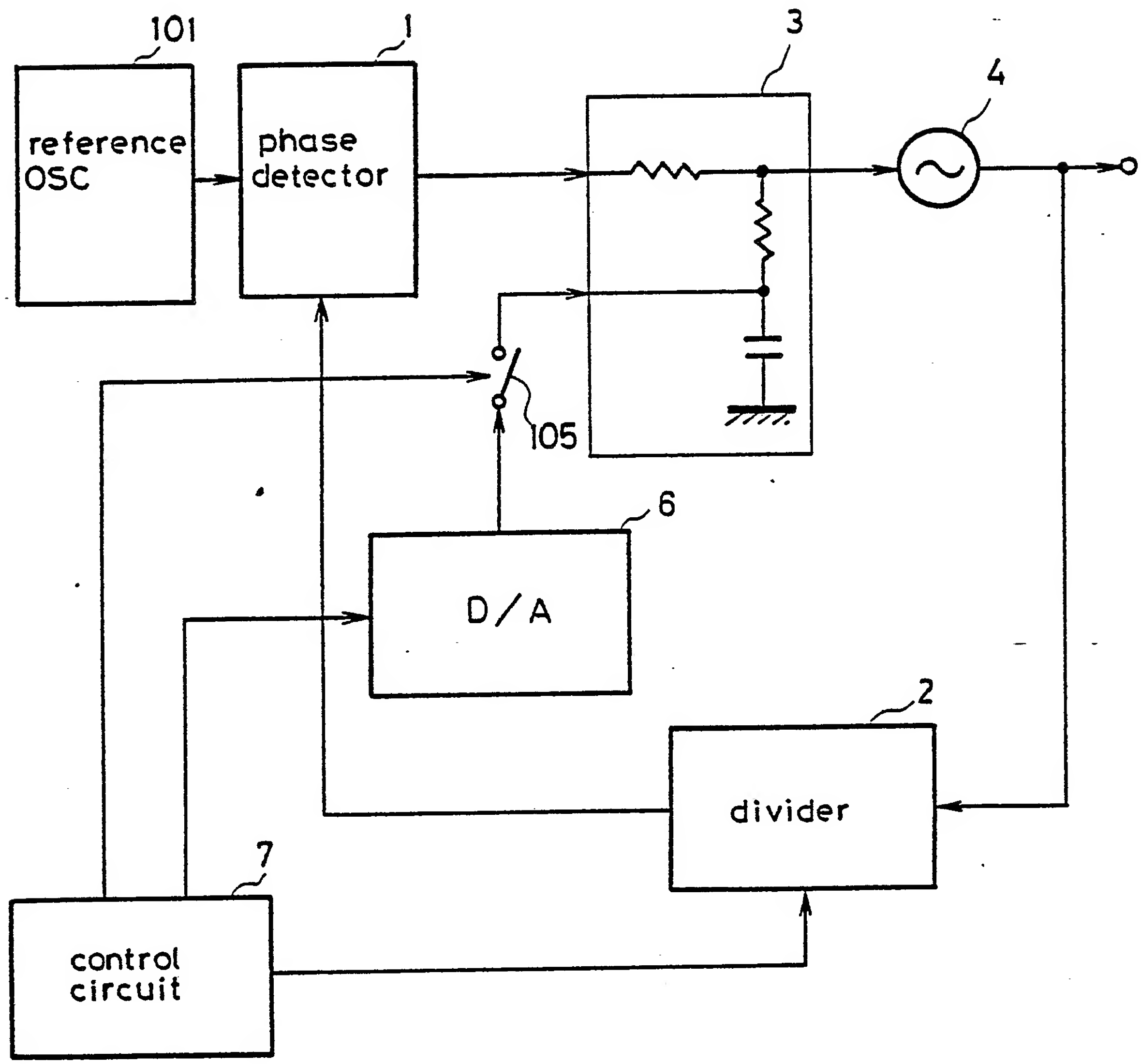

101
1
3
4
reference OSC
phase detector
105
6
D/A
2
divider
7
control circuit

FIG. 22

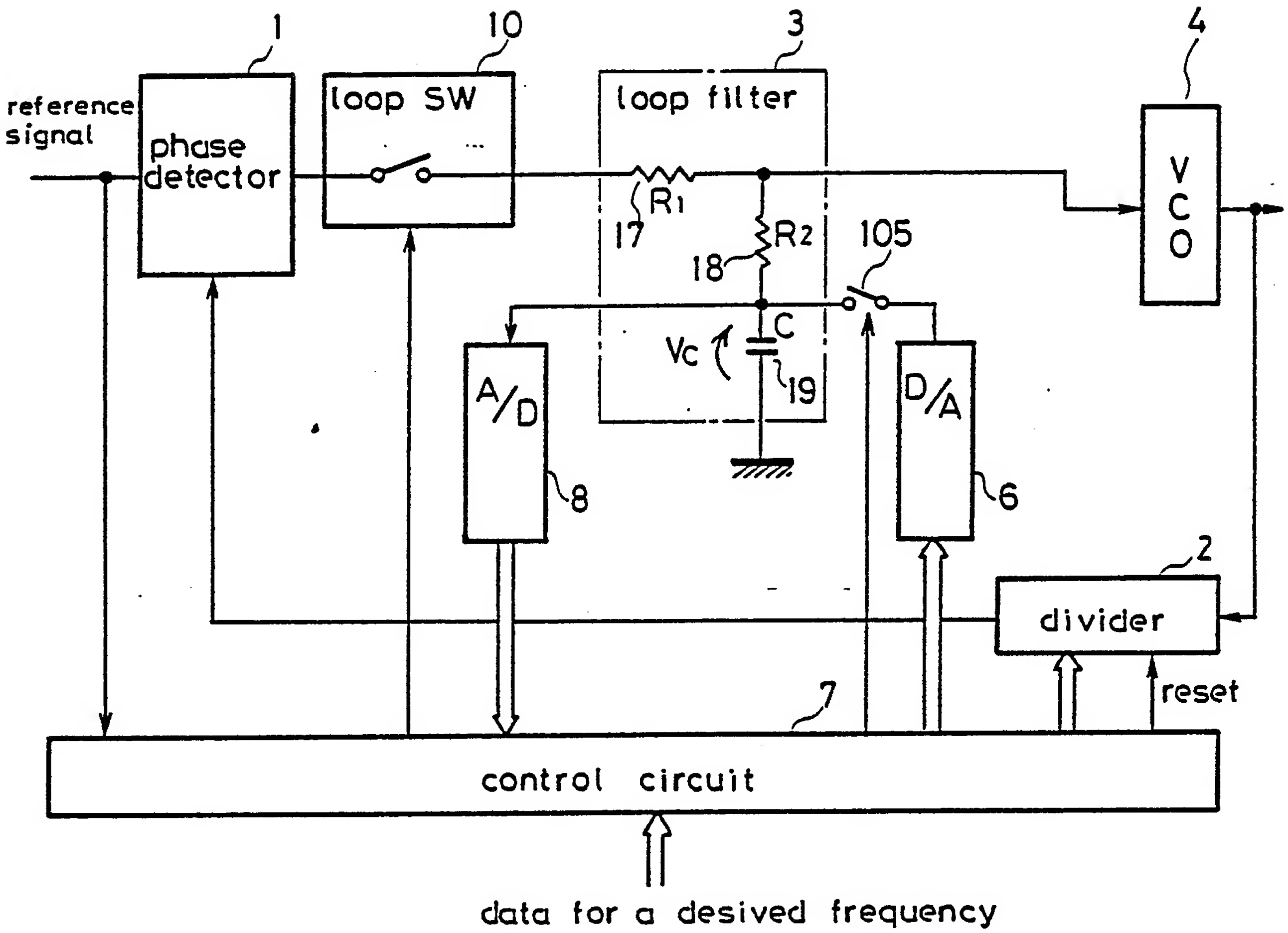

1
10
3
4
reference signal
phase detector
loop SW
loop filter
R1
17
R2
18
105
C
Vc
19
V C O
A/D
D/A
8
6
2
divider
reset
7
control circuit
data for a desived frequency

FIG. 23

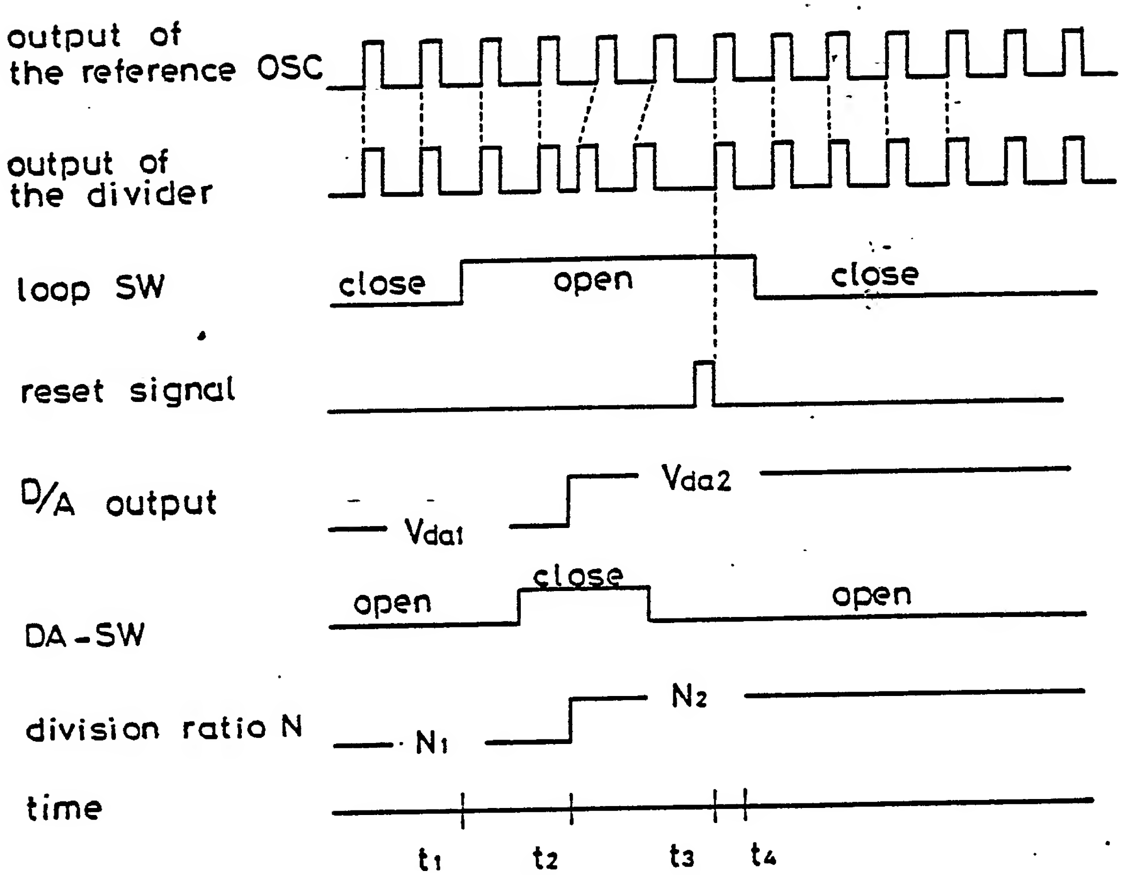

output of
the reference OSC
output of
the divider
loop SW
close
open
close
reset signal
D/A output
Vda1
Vda2
DA-SW
open
close
open
division ratio N
N1
N2
time
t1
t2
t3
t4

FIG. 24

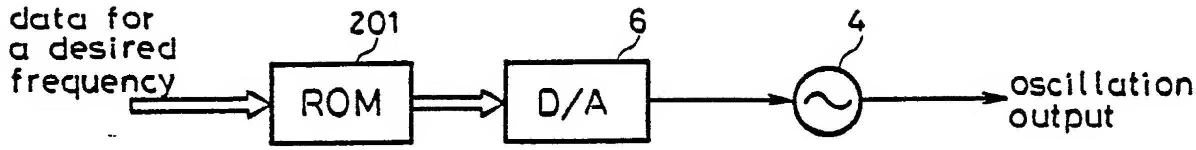



FIG.25

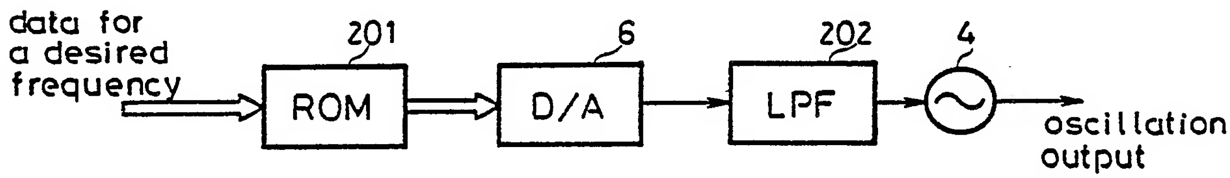



FIG. 26

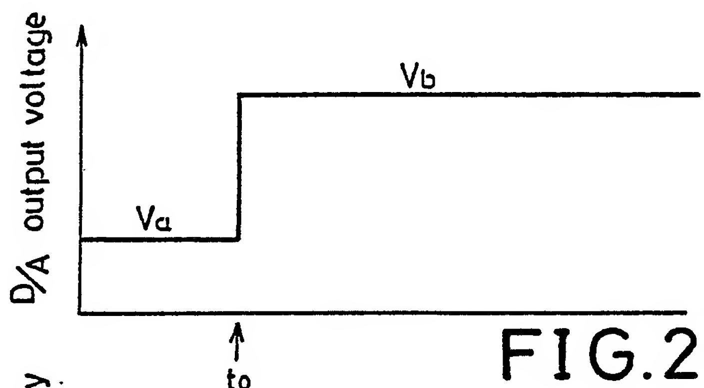



FIG.27(a)

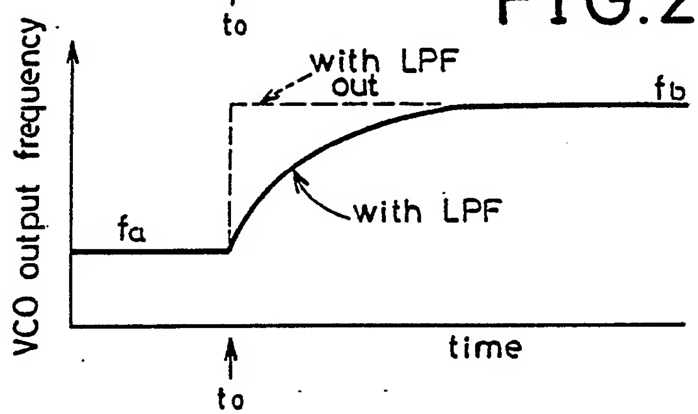



FIG. 27(b)

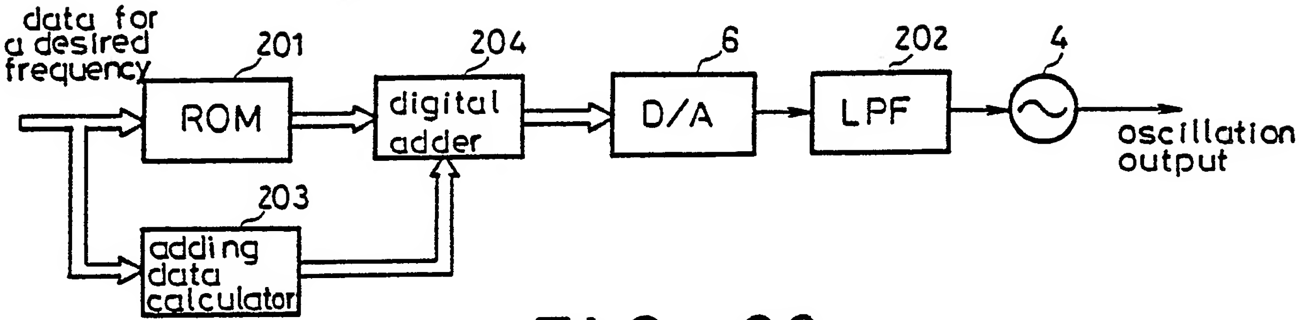



FIG. 28

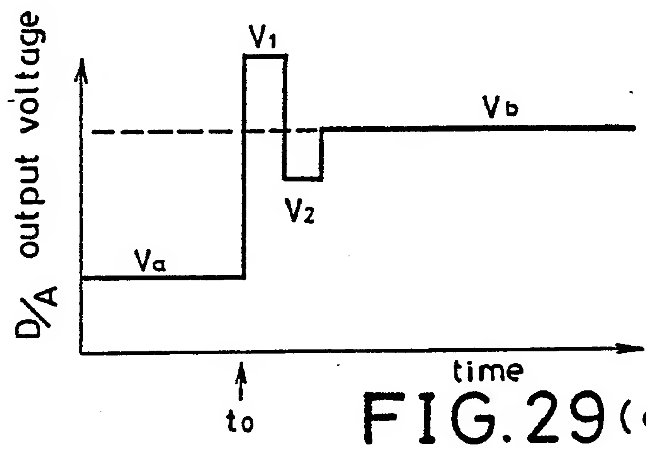



FIG. 29(a)

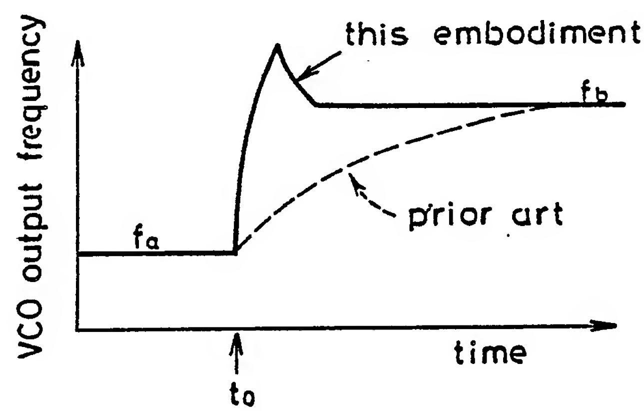



FIG. 29(b)

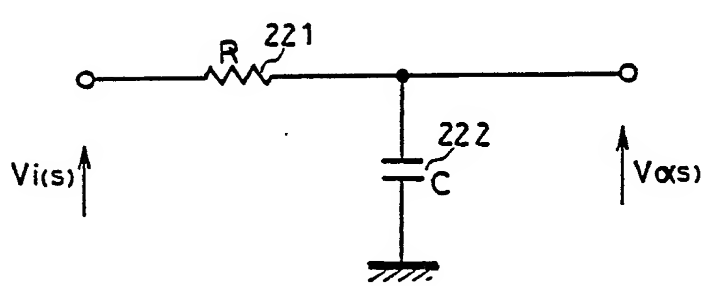



FIG. 30

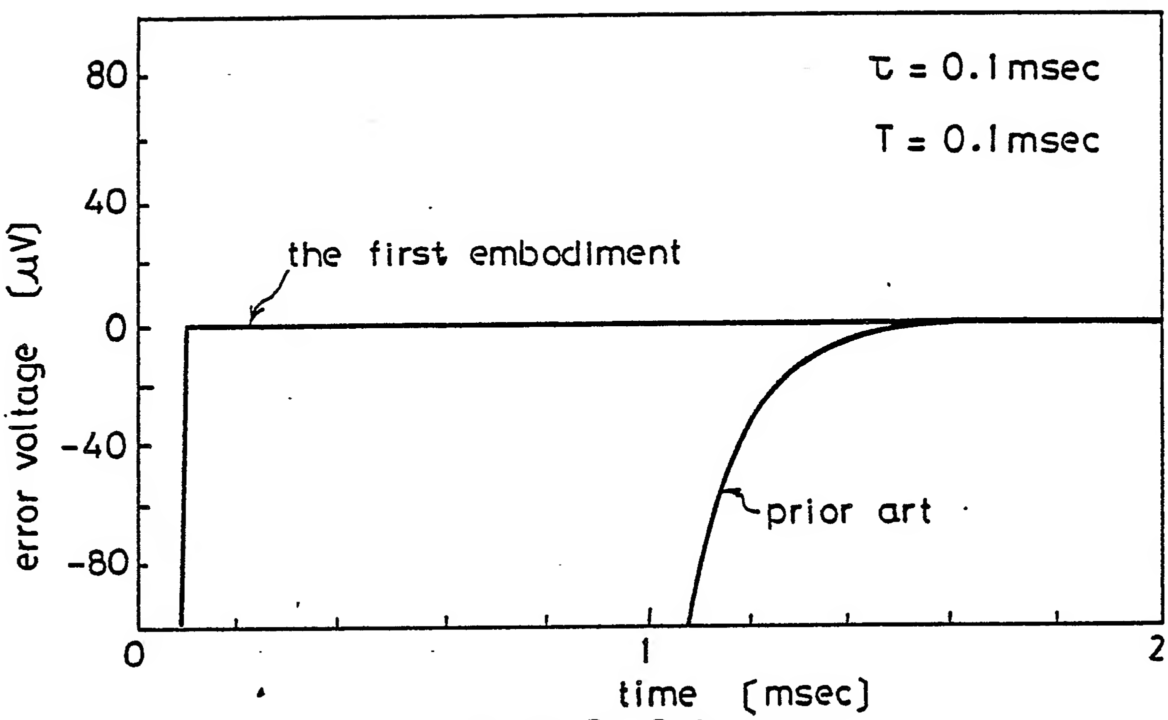



FIG.31(a)

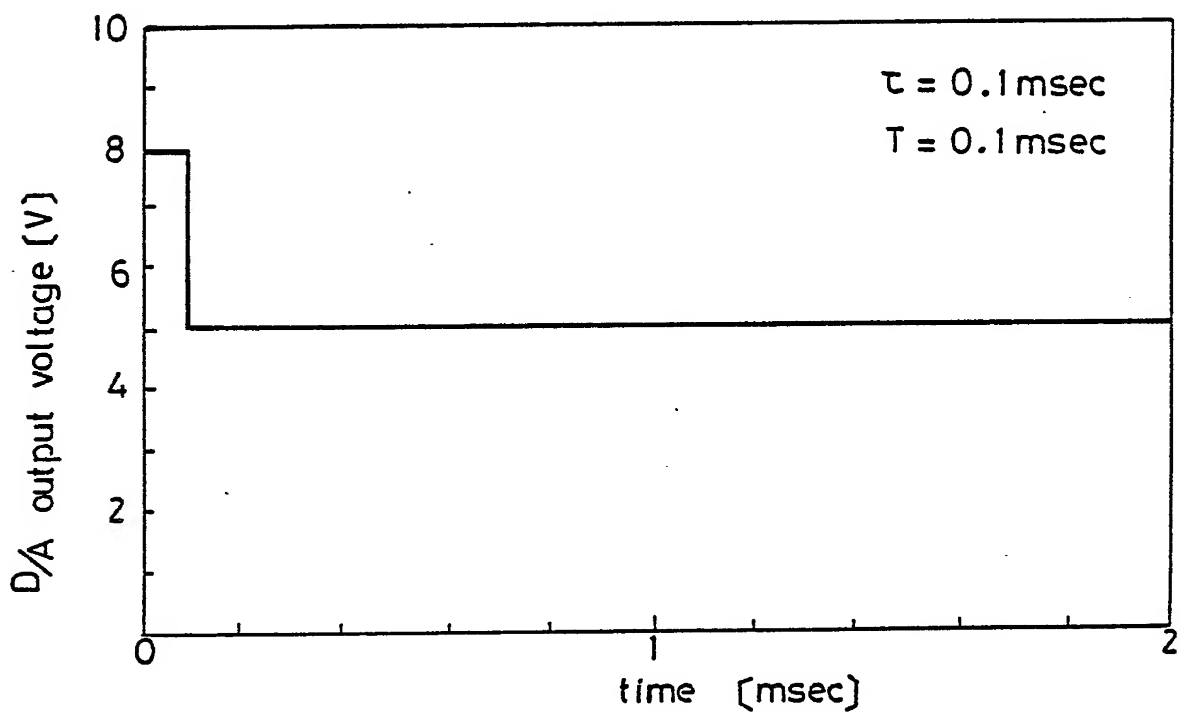



FIG. 31(b)

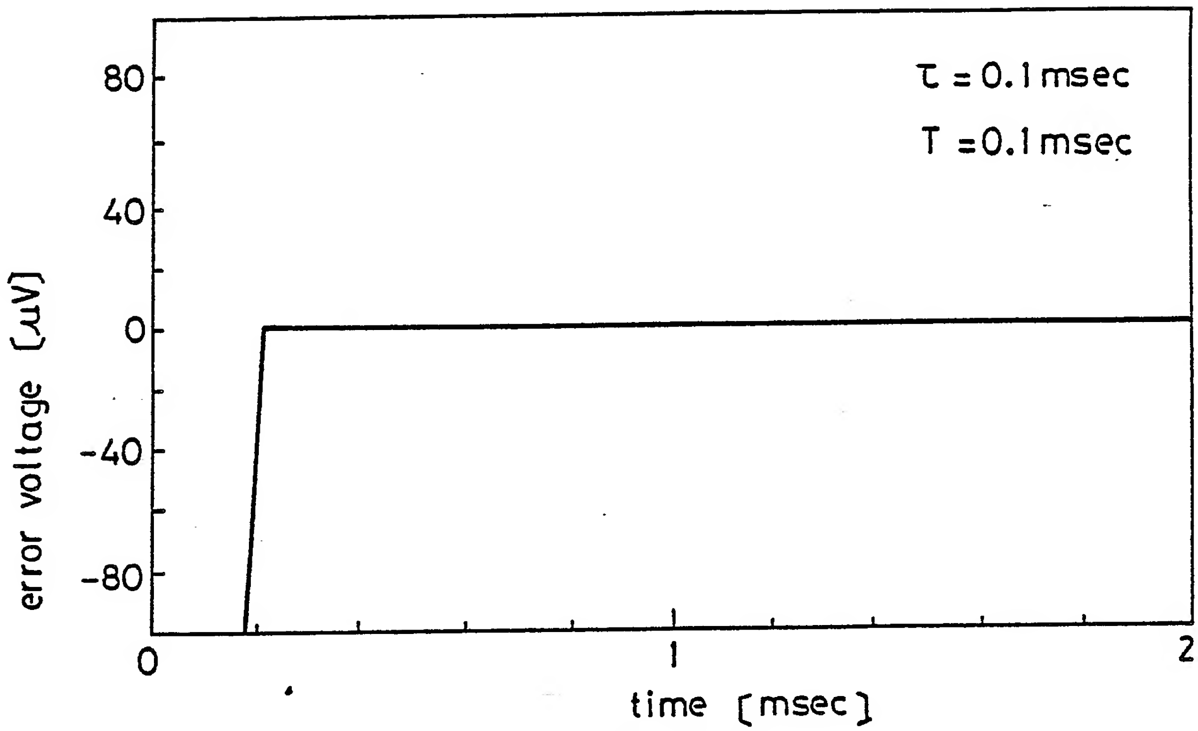



FIG.32(a)

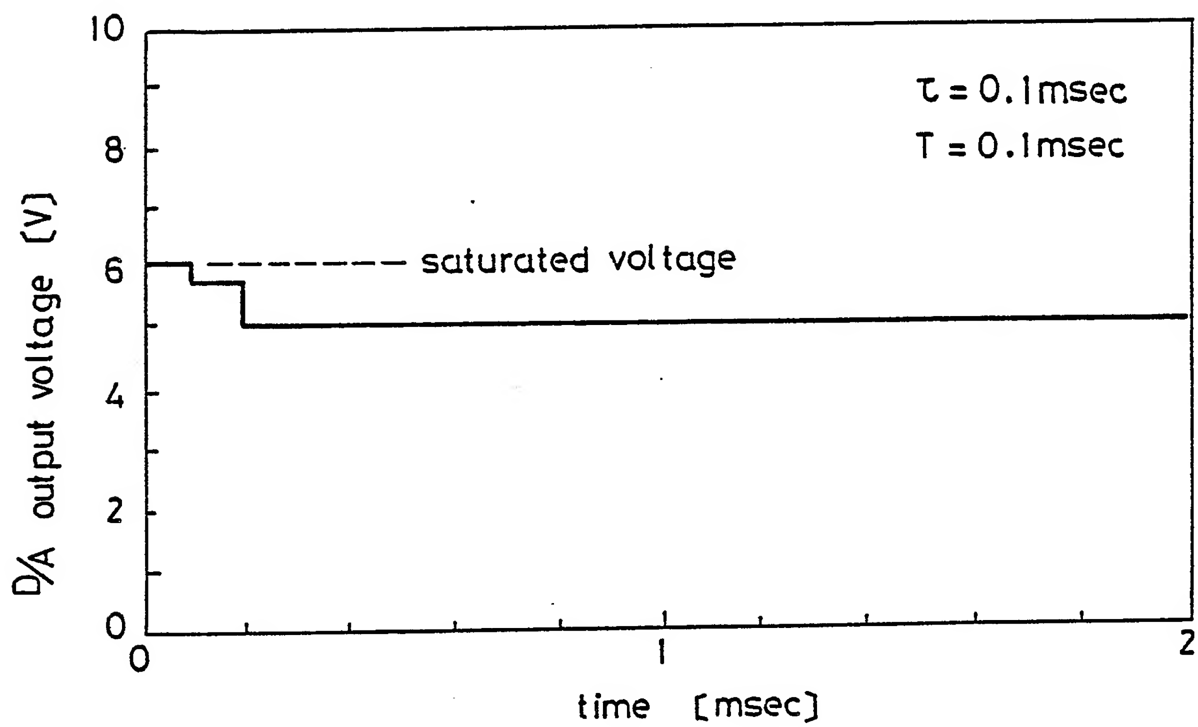



FIG. 32(b)

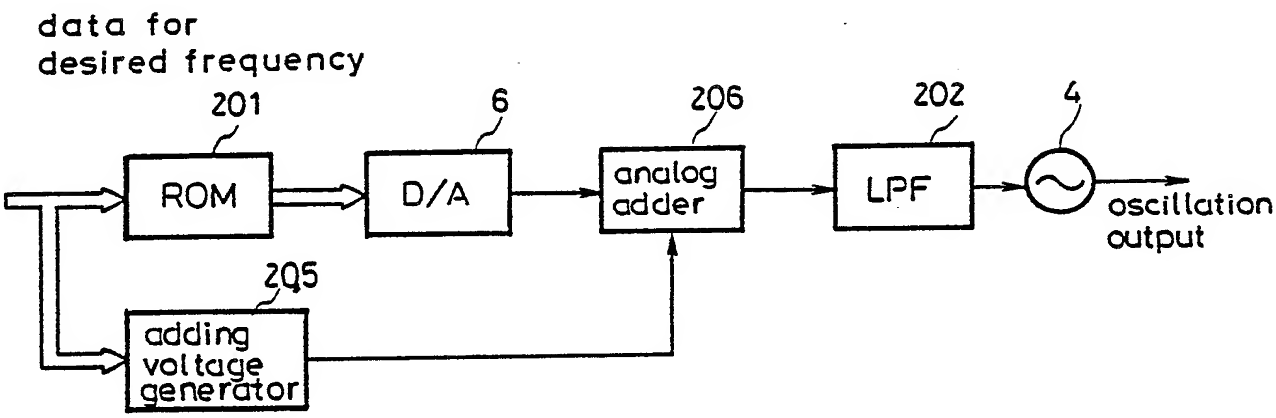

data for
desired frequency
201
ROM
6
D/A
206
analog
adder
202
LPF
4
oscillation
output
205
adding
voltage
generator

FIG. 33

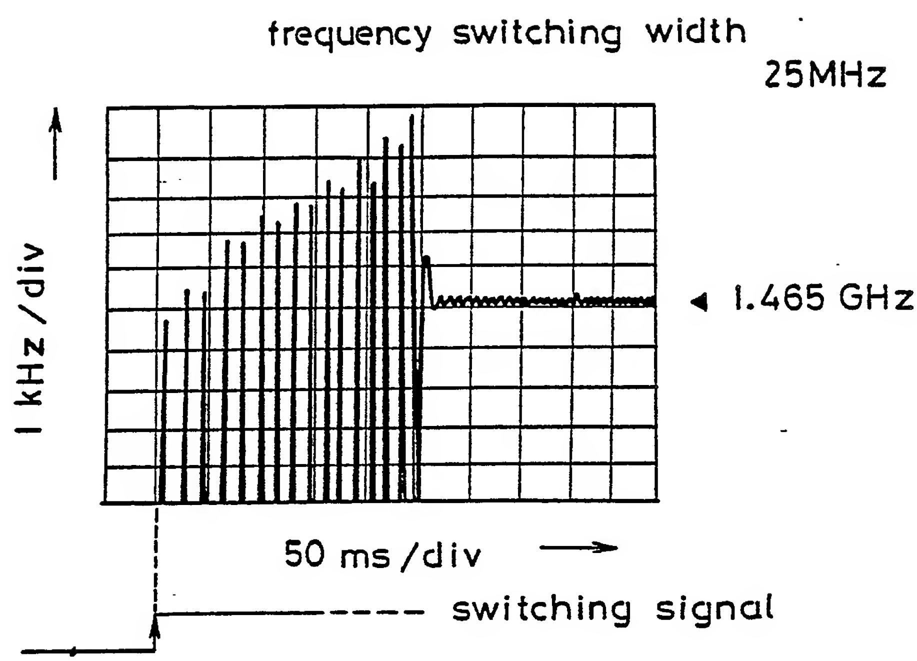

frequency switching width
25MHz
1 kHz /div
1.465 GHz
50 ms /div
switching signal

FIG. 34

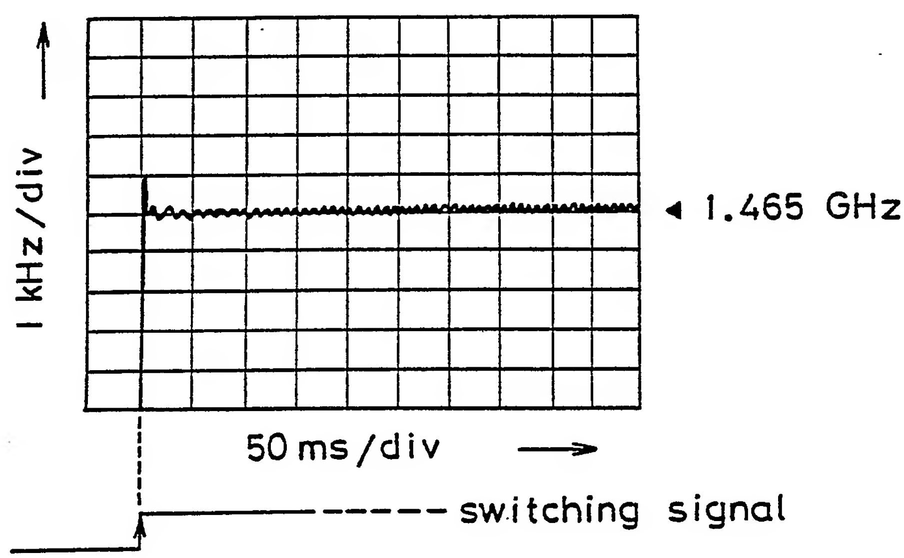

1 kHz /div
1.465 GHz
50 ms /div
switching signal

FIG. 35

European Patent Office

# EUROPEAN SEARCH REPORT

Application Number

EP 89 30 8858

## DOCUMENTS CONSIDERED TO BE RELEVANT

| Category | Citation of document with indication, where appropriate, of relevant passages | Relevant to claim | CLASSIFICATION OF THE APPLICATION (Int. Cl.5) |
|---|---|---|---|
| X | EP-A-0 041 882 (THOMSON-CSF)<br>* Page 1, line 1 - page 3, line 25; page 6, line 1 - page 17, line 32; figures 3-9 * | 1-4,7-12,15-19 | H 03 L 7/189<br>H 03 L 7/14 |
| Y | | 5,6,13,14 | |
| X | US-A-4 410 860 (KIPP et al.)<br>* Whole document * | 1-4,7-12,15-19 | |
| Y | | 5,6,13,14 | |
| Y | FR-A-2 356 332 (INDESIT)<br>* Page 5, line 7 - page 6, line 14; figure 1 * | 5,6,13,14 | |

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

H 03 L

The present search report has been drawn up for all claims

| Place of search | Date of completion of the search | Examiner |
|---|---|---|
| THE HAGUE | 21-12-1989 | DHONDT I.E.E. |

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document